

FIG. 2 PRIOR ART

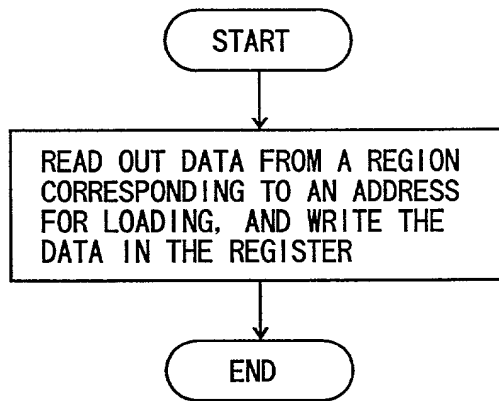


FIG. 3 PRIOR ART

OP-CODE	GR1	GR2	GRD
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FIG. 4 PRIOR ART

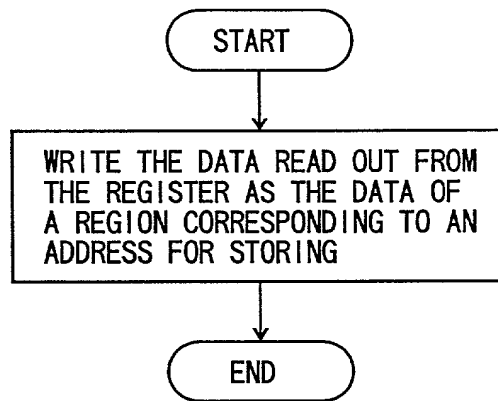


FIG. 5 PRIOR ART

OP-CODE	GR1	GR2	GRS
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FIG. 6 PRIOR ART

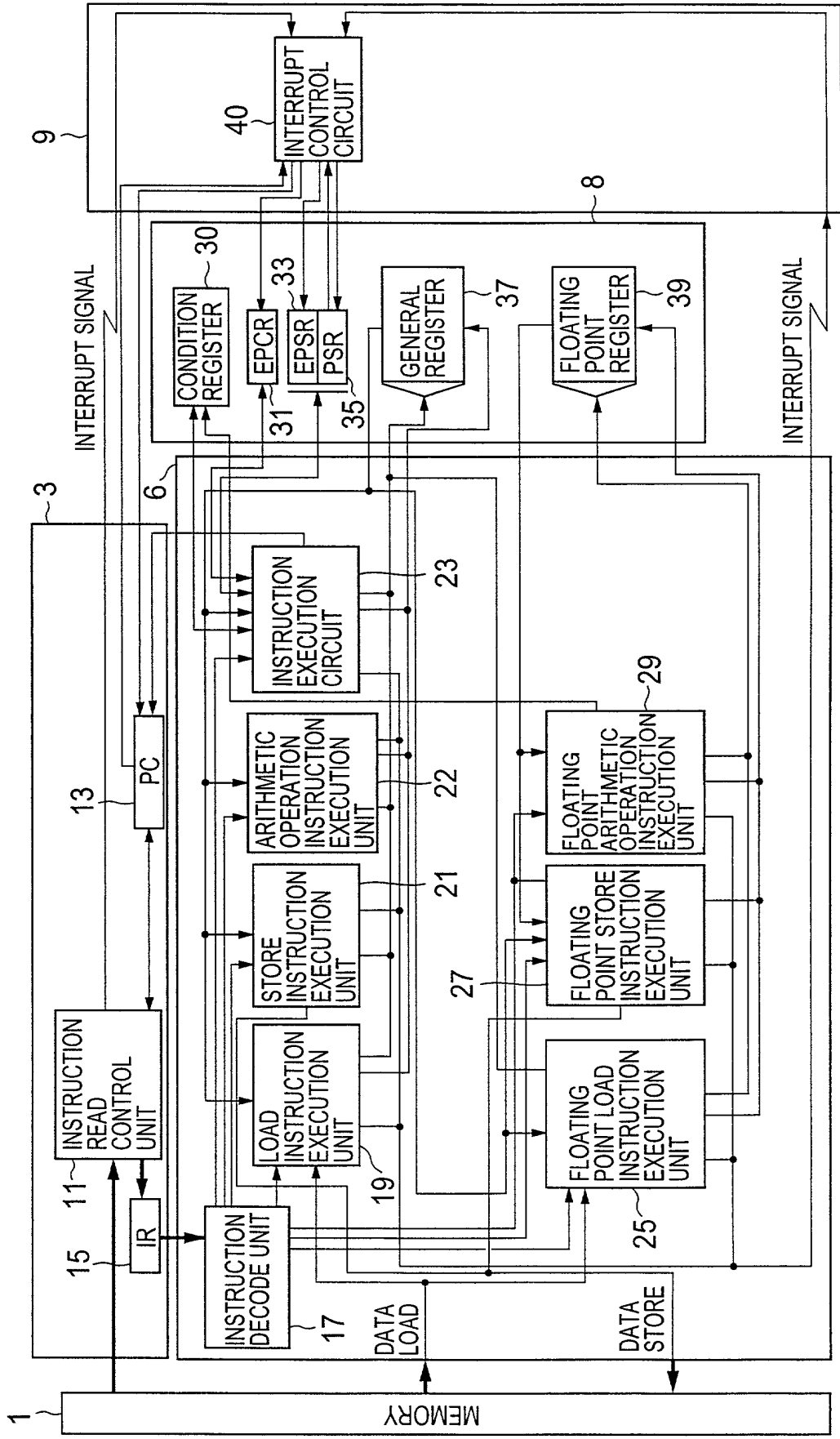
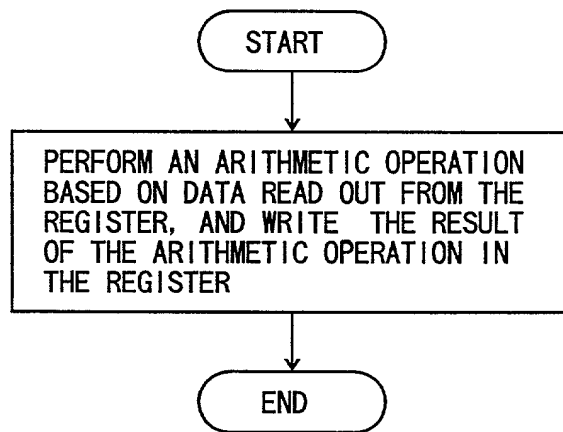


FIG. 7 PRIOR ART



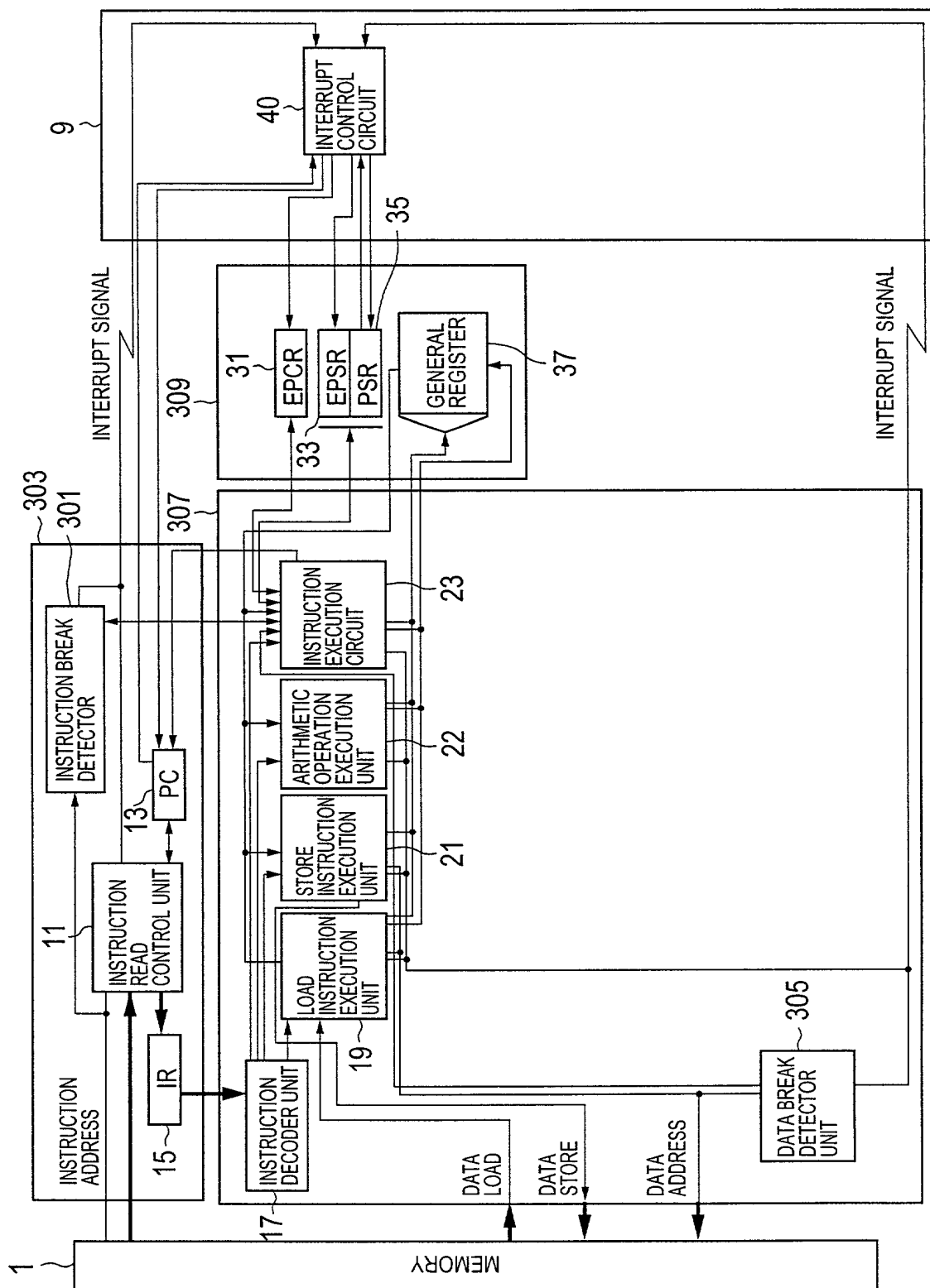
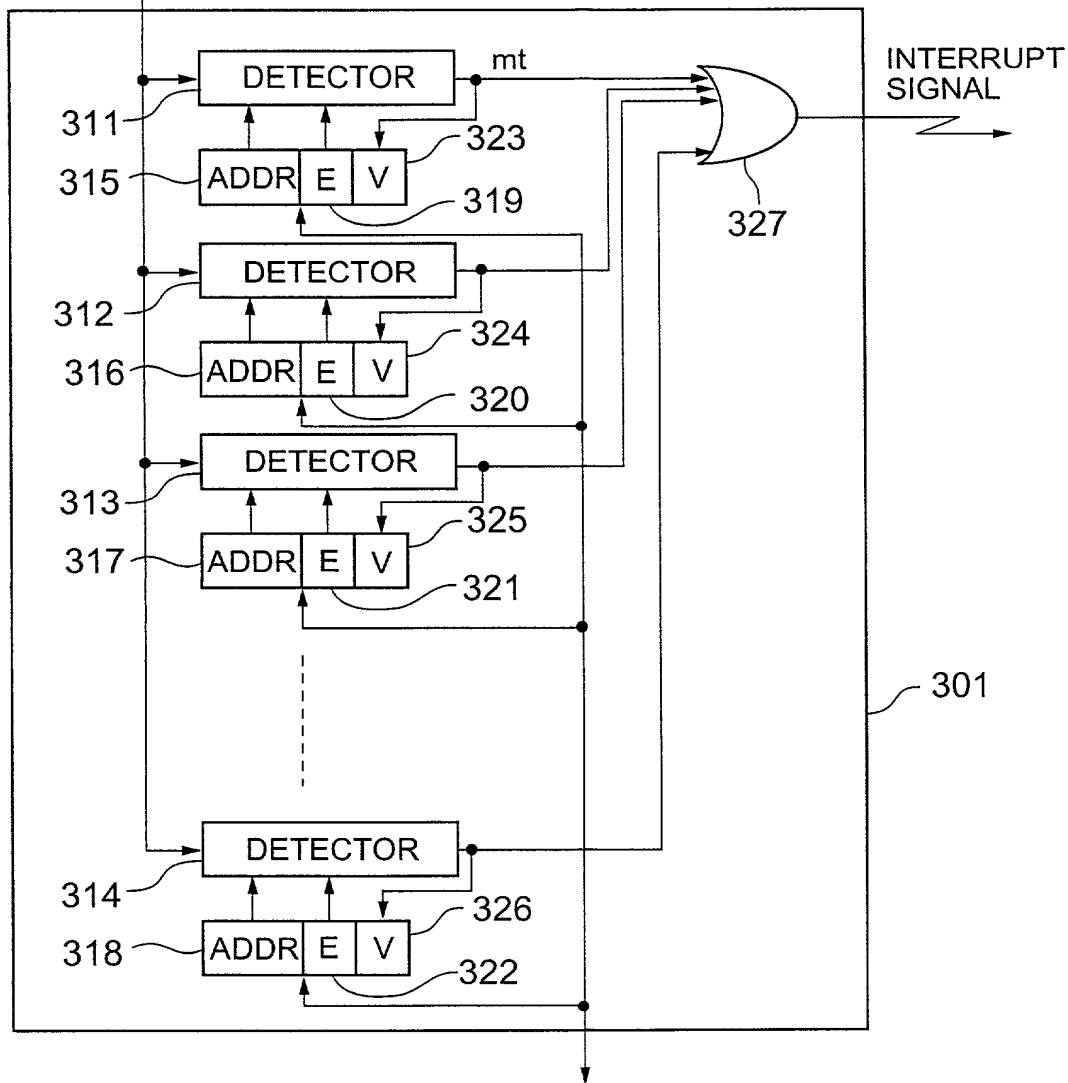


FIG.9 PRIOR ART

INSTRUCTION ADDRESS



TO THE INSTRUCTION EXECUTION CIRCUIT

FIG.10 PRIOR ART

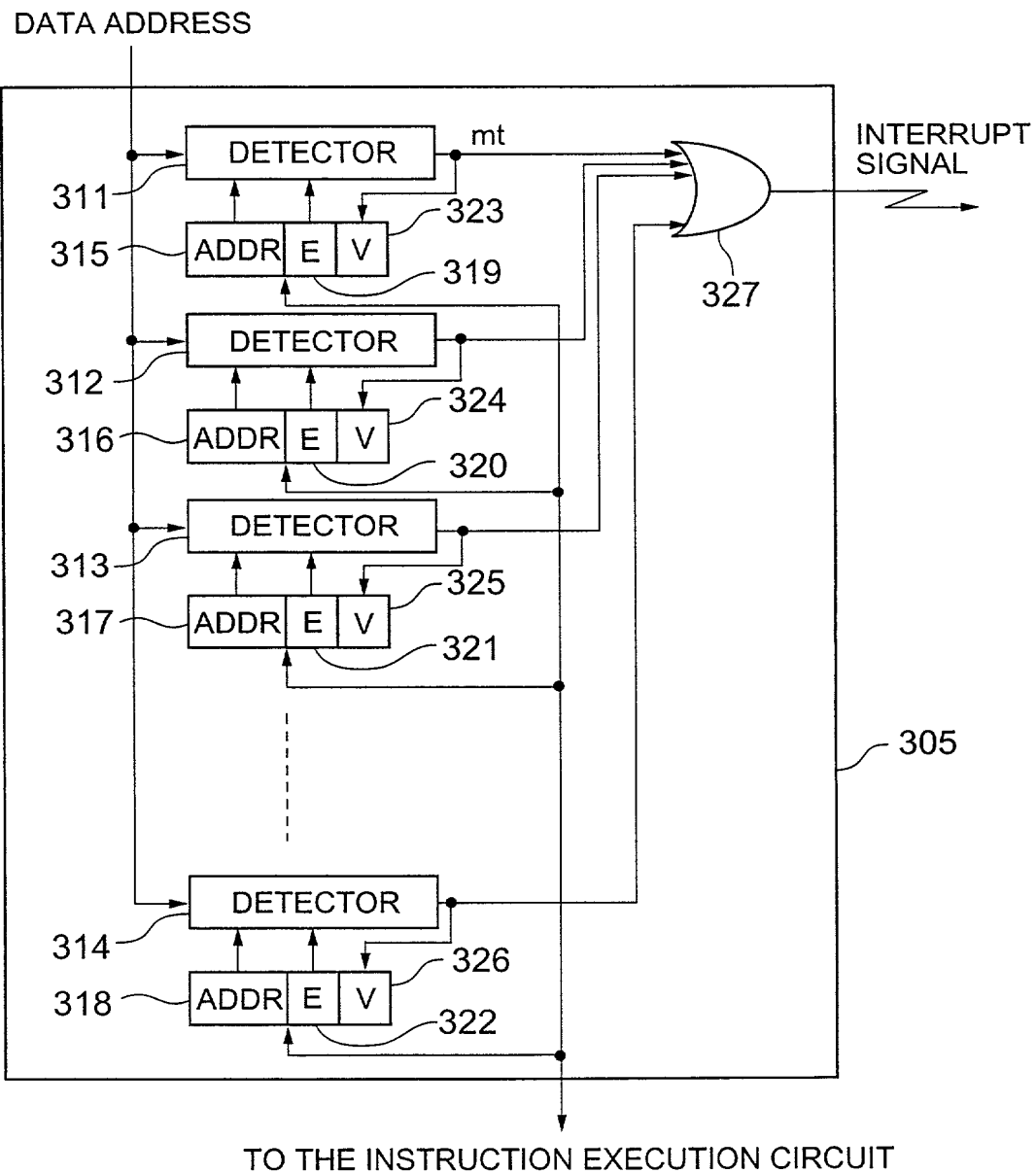


FIG.11 PRIOR ART

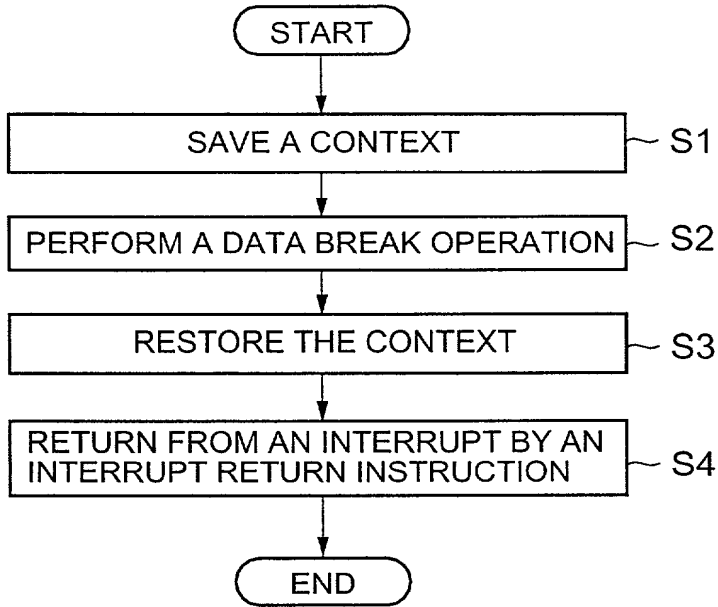


FIG.12 PRIOR ART

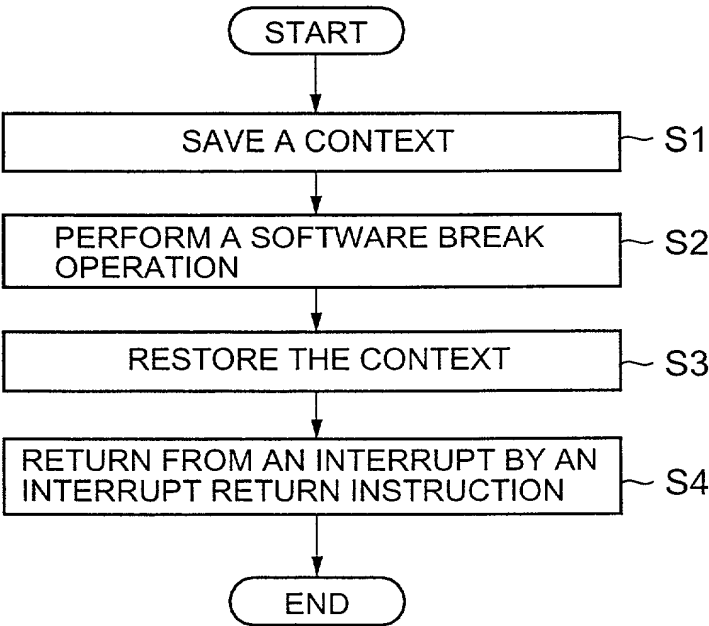


FIG. 13

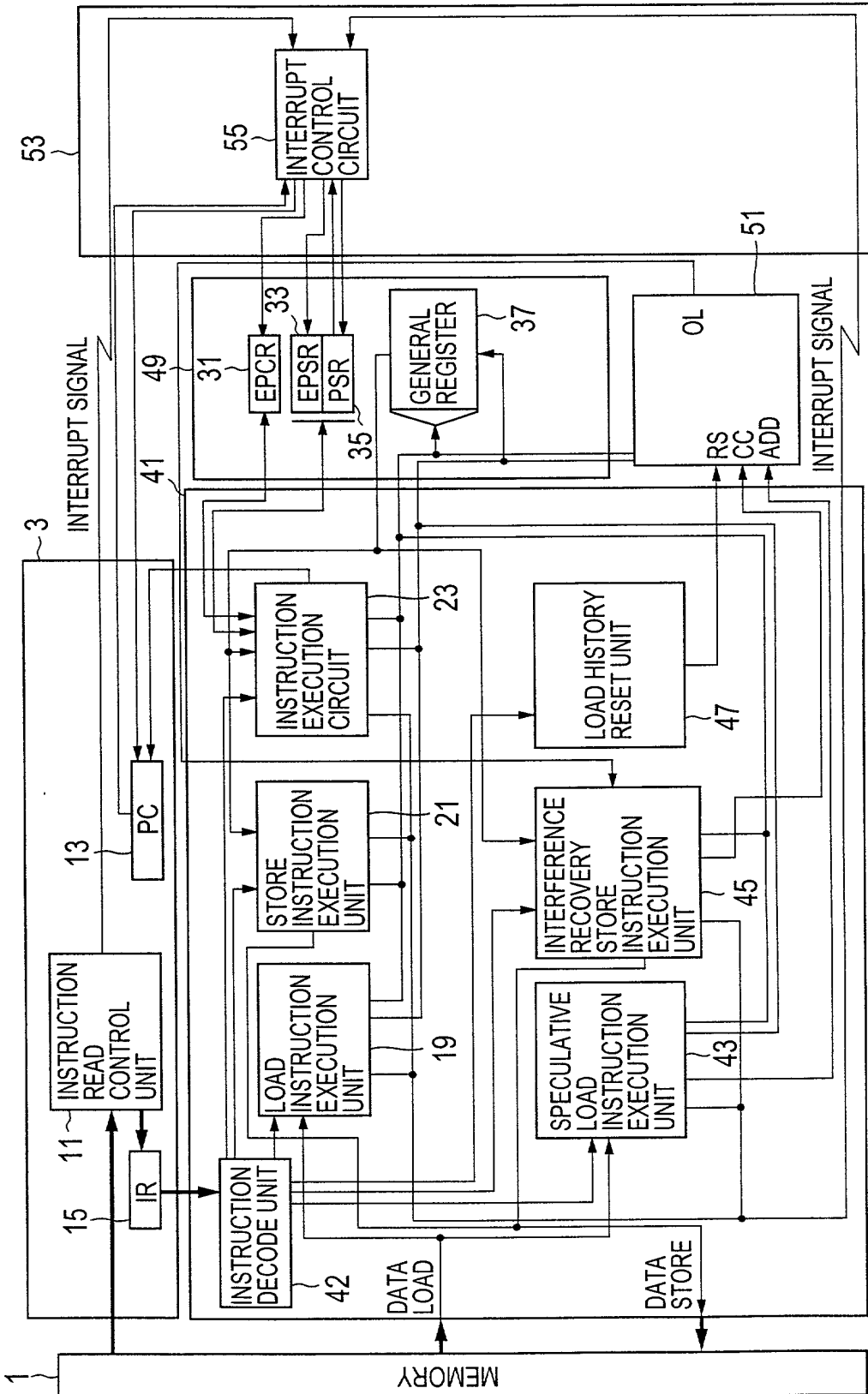


FIG. 14

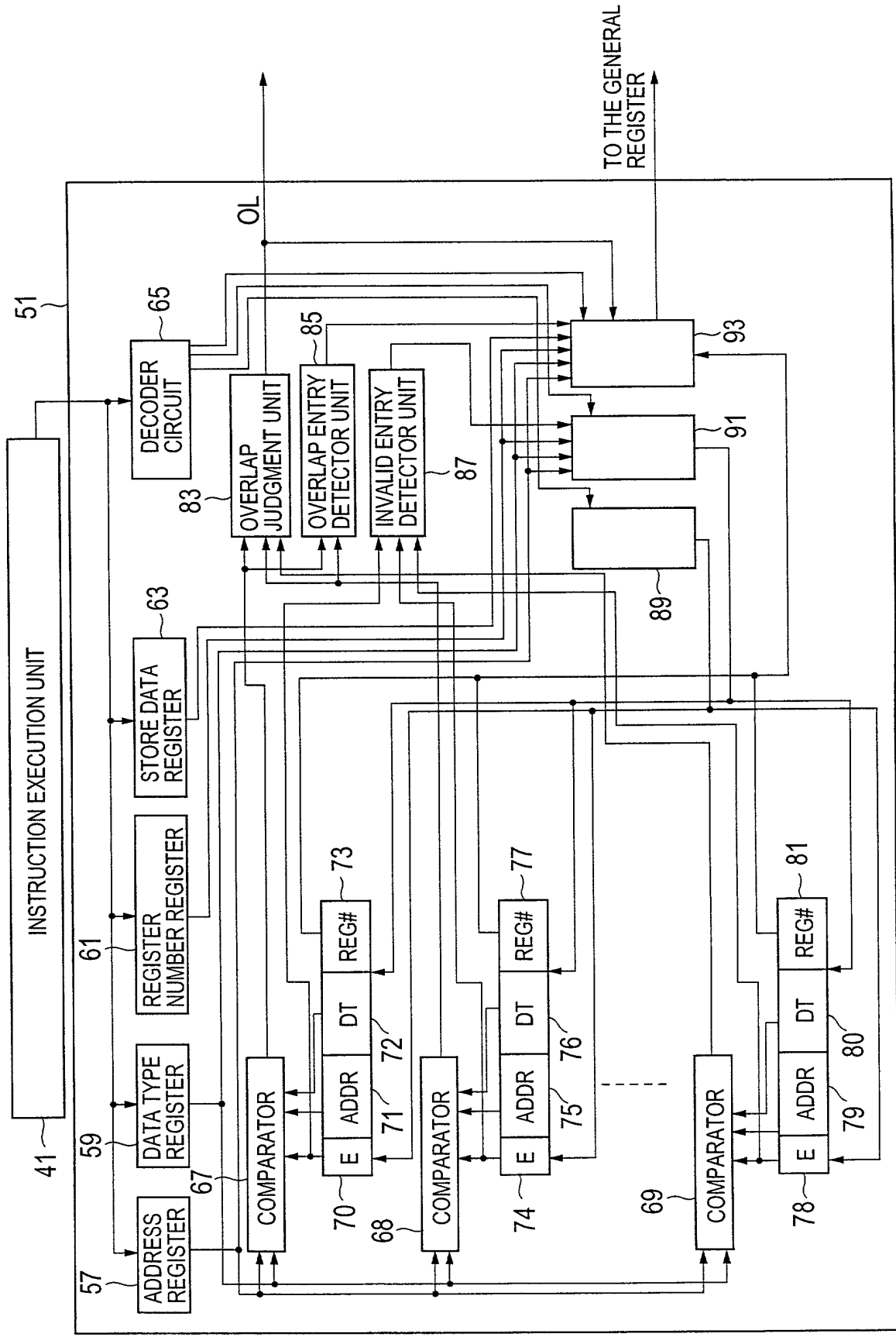


FIG. 15

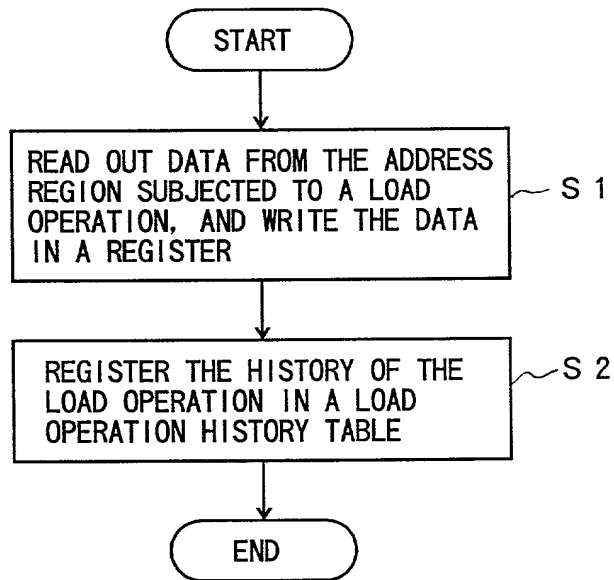


FIG. 16

OP-CODE	GR1	GR2	GRD
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FIG. 17

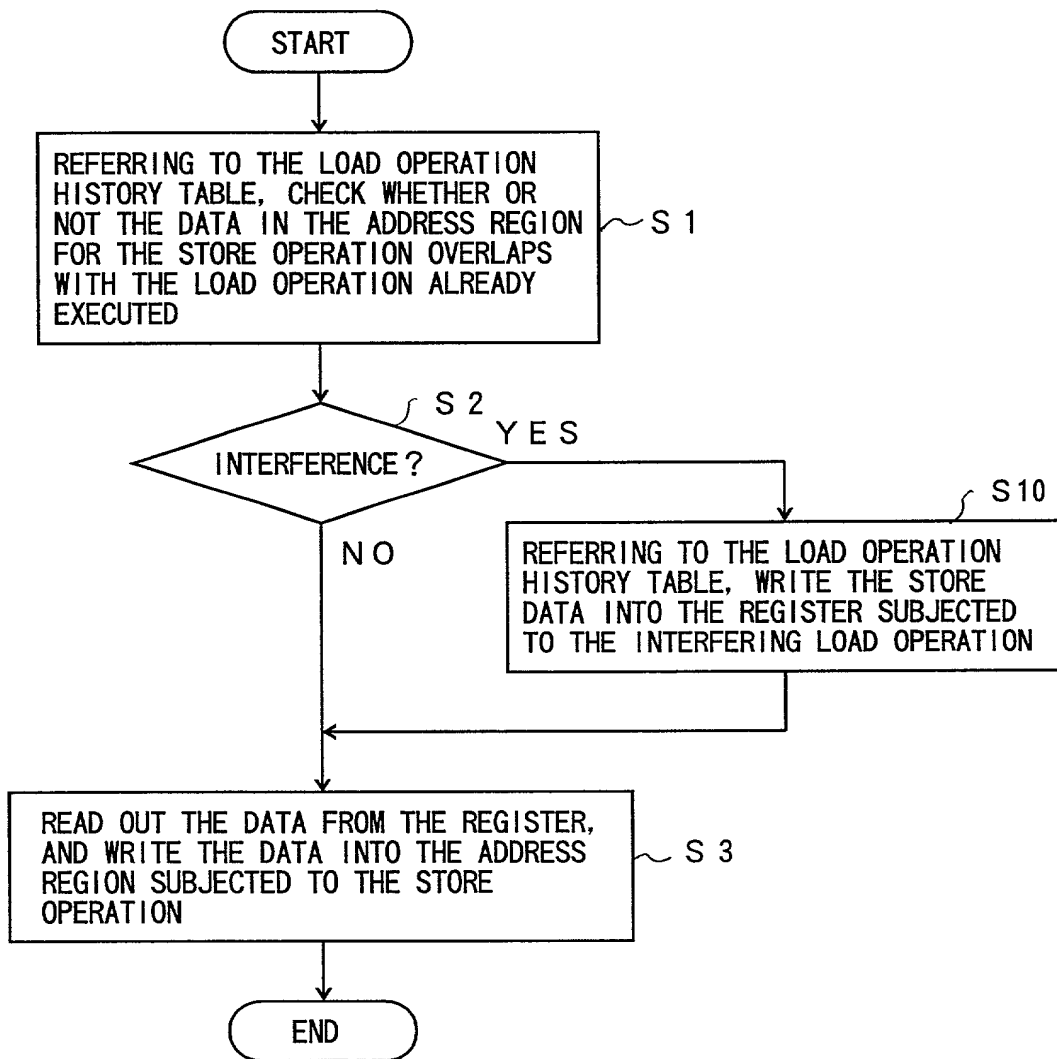


FIG. 18

OP-CODE	GR1	GR2	GRS
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FIG. 19

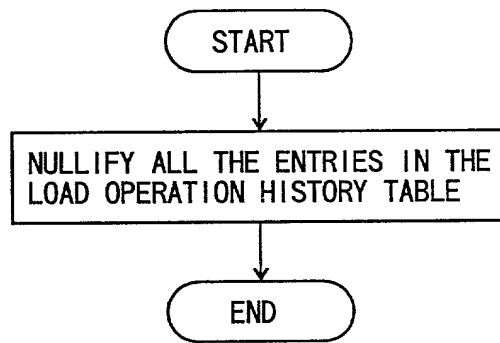
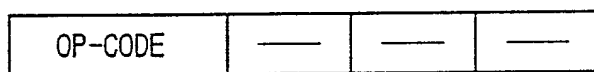


FIG. 20



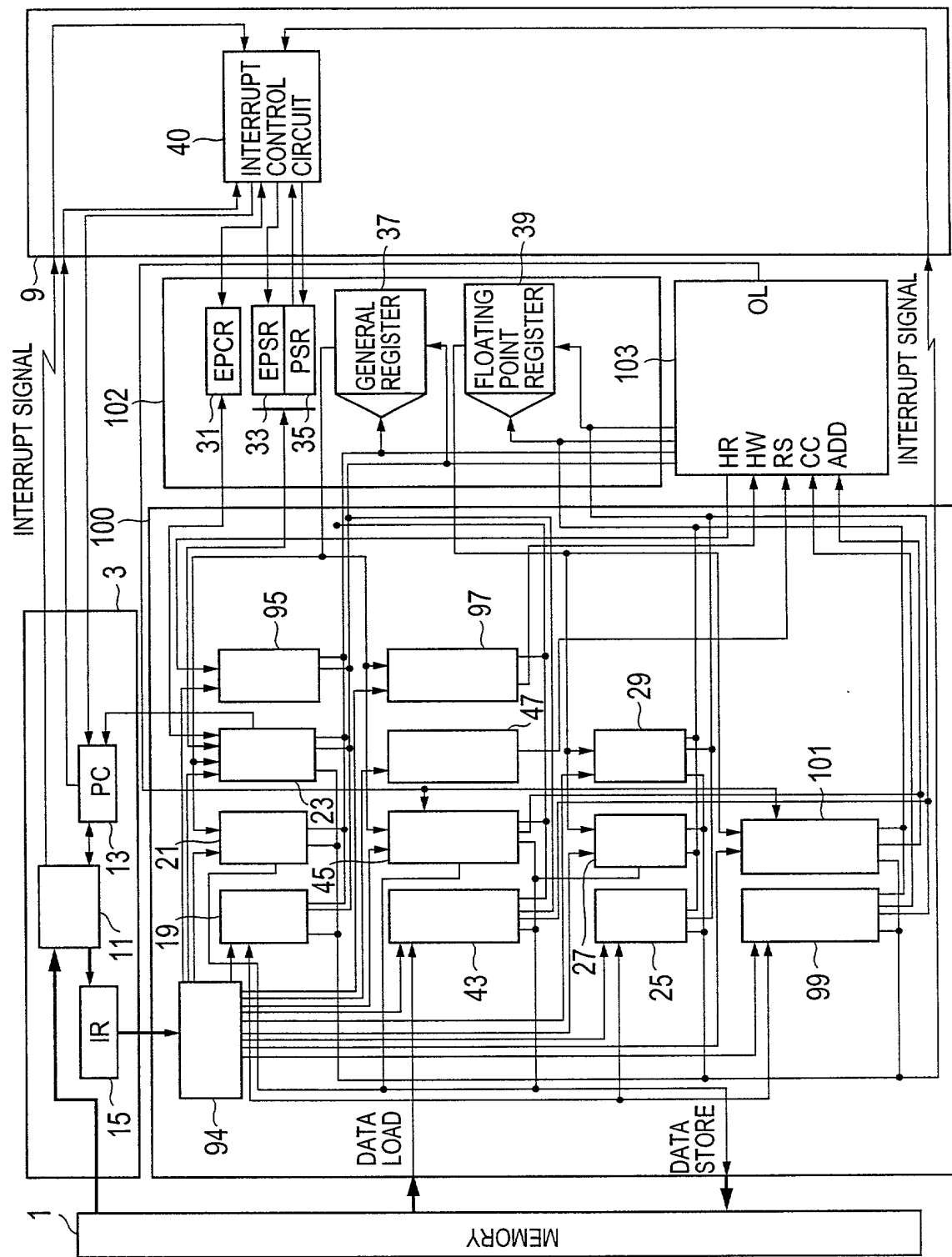


FIG. 22

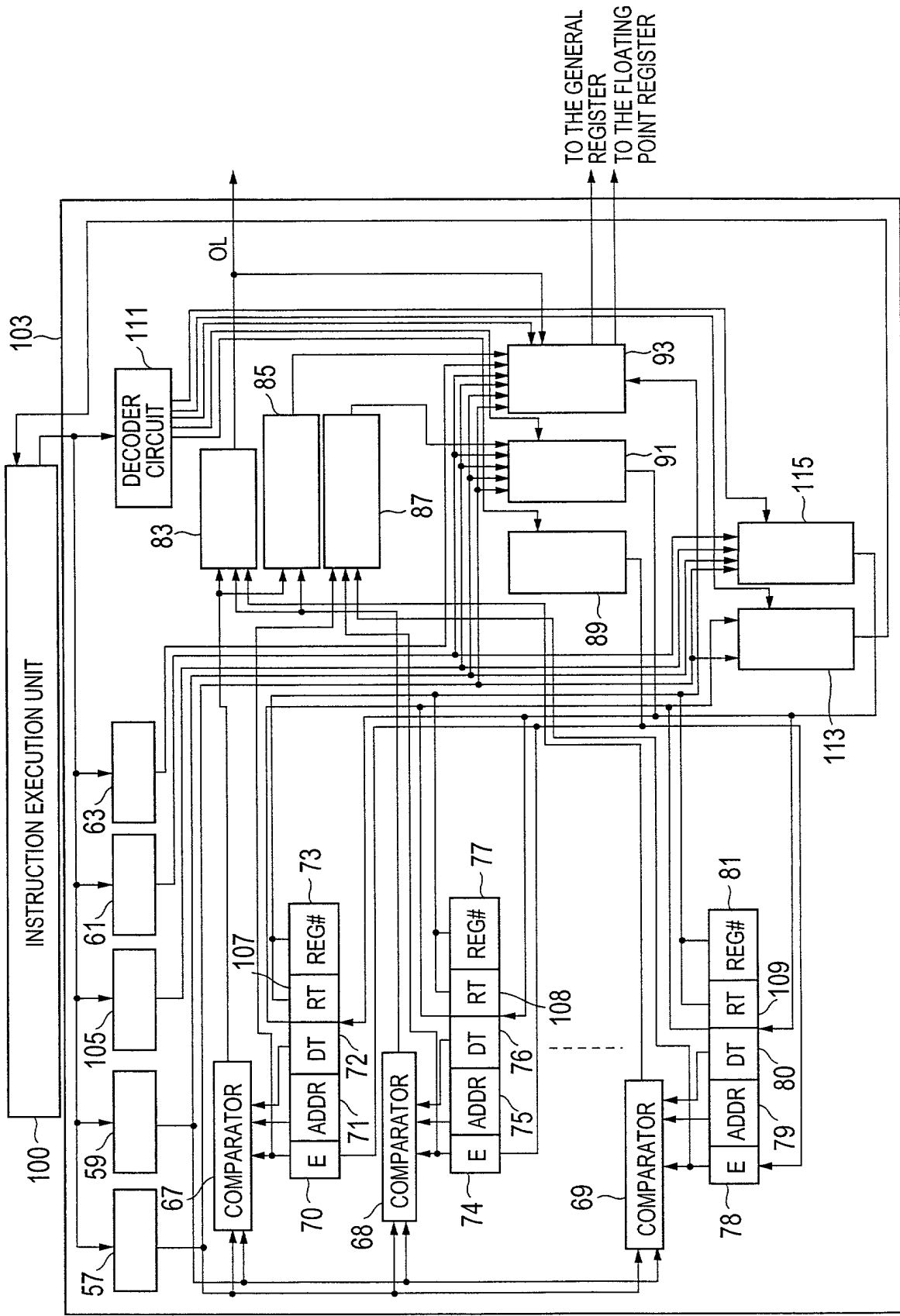


FIG. 24

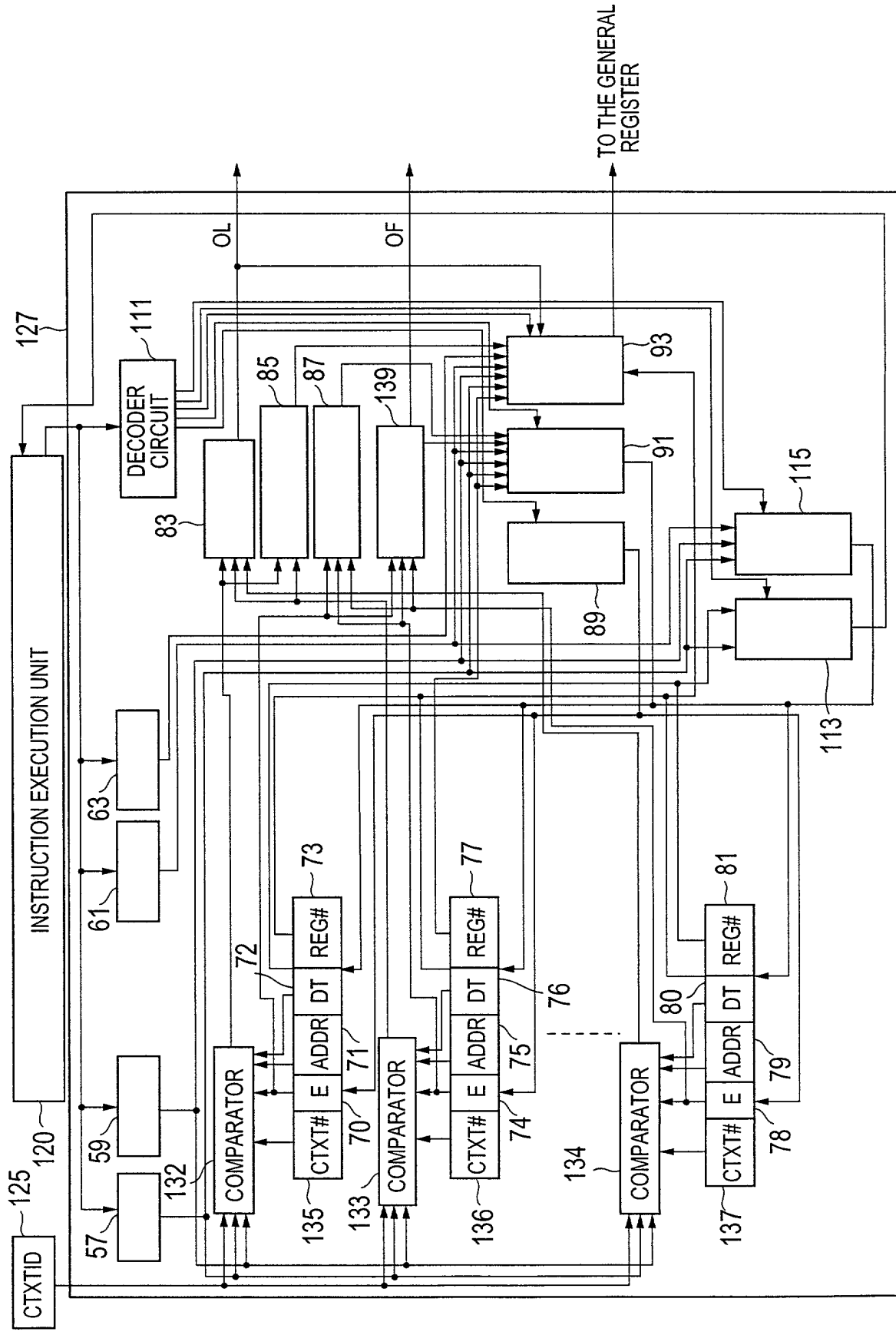


FIG. 25

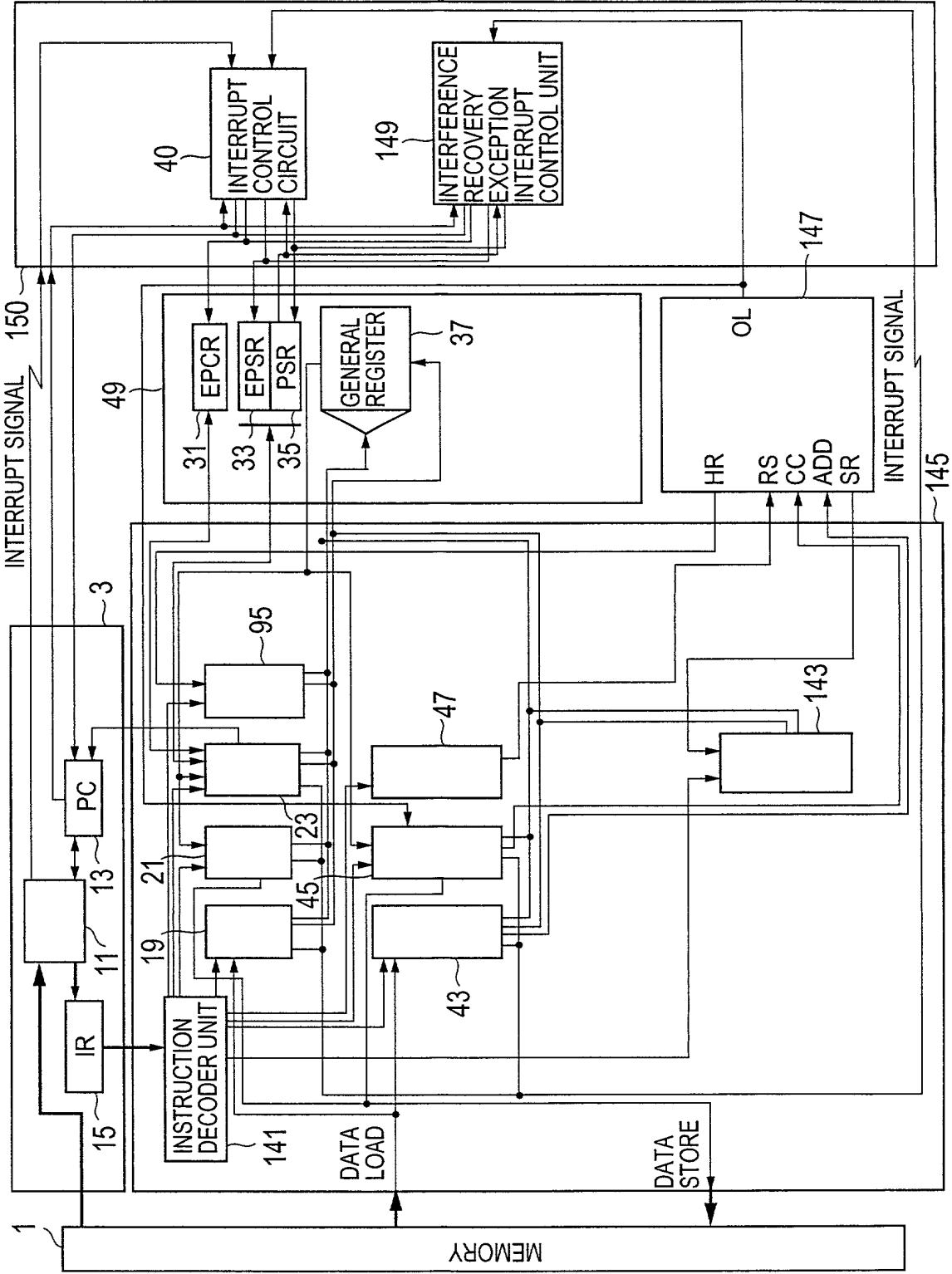


FIG. 26

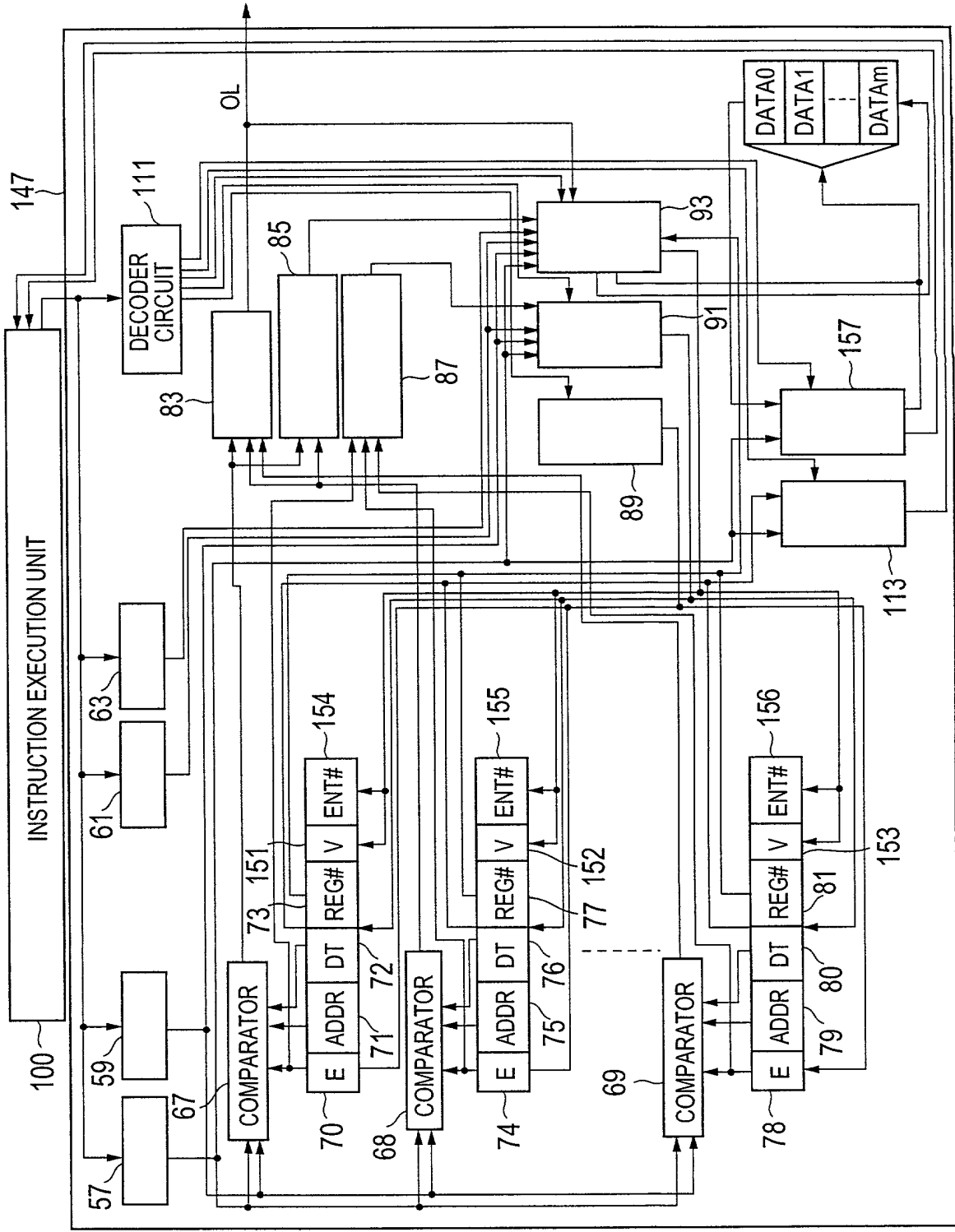


FIG. 27

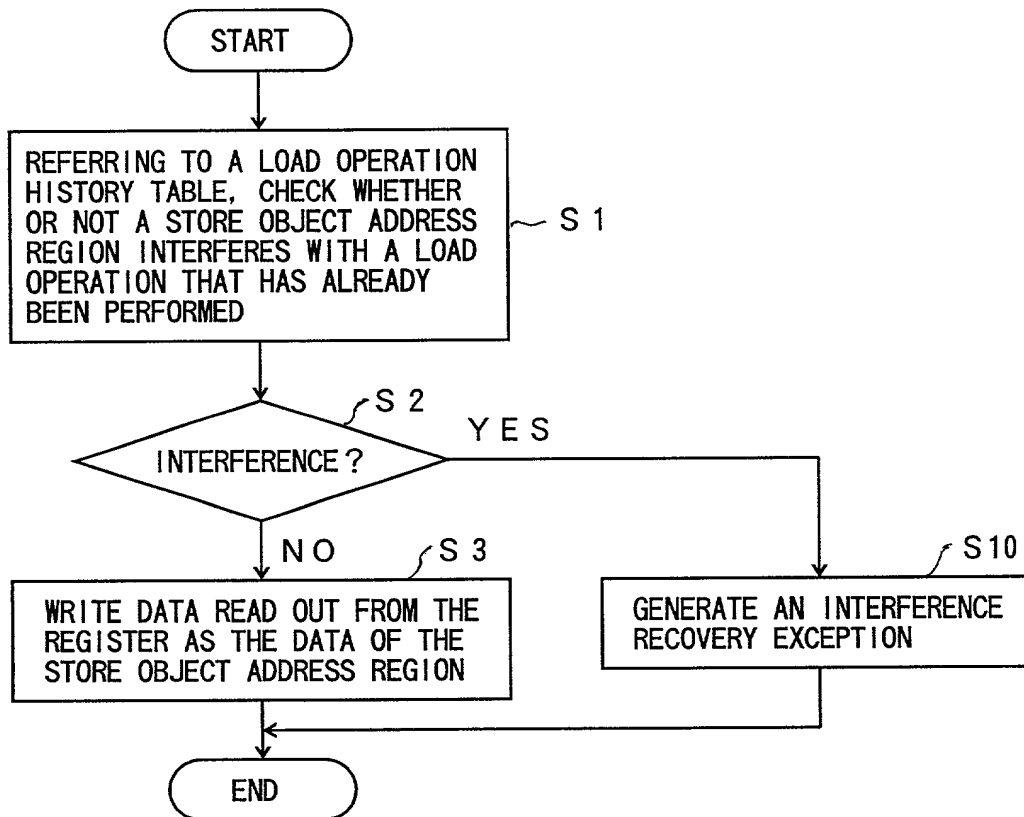


FIG. 28

OP-CODE	GR1	GR2	GRS
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FIG. 29

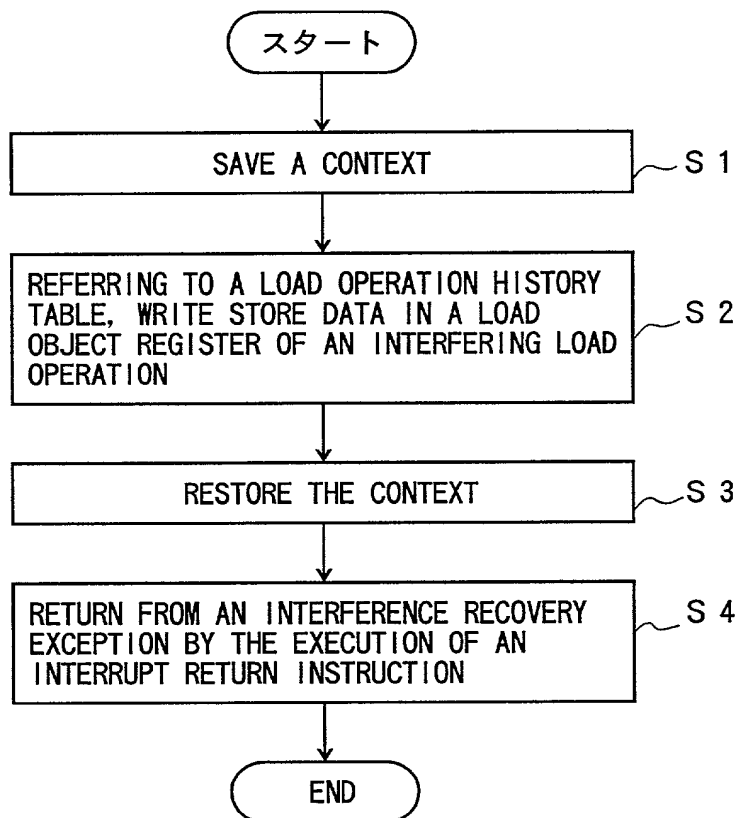


FIG. 30

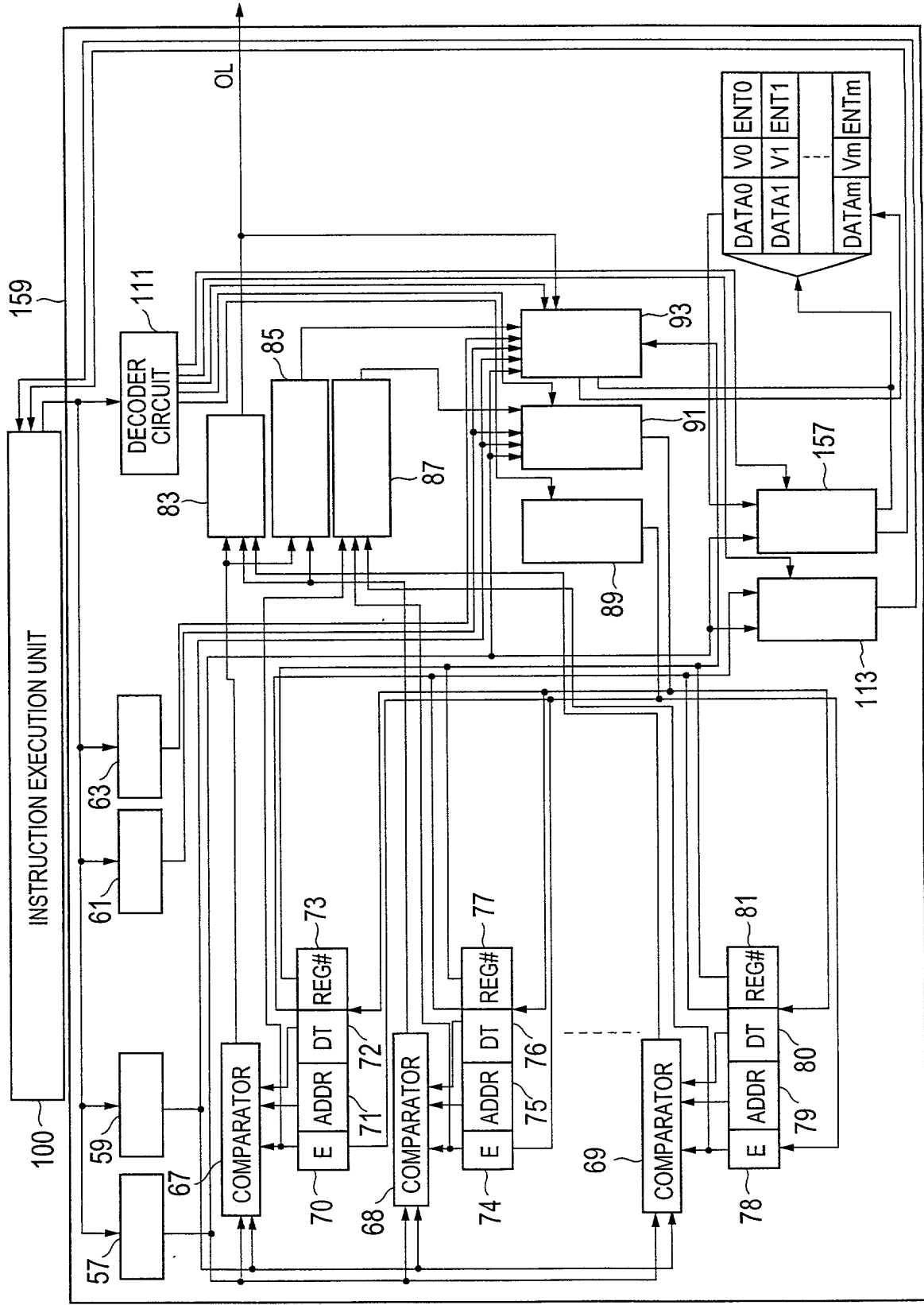


FIG. 31

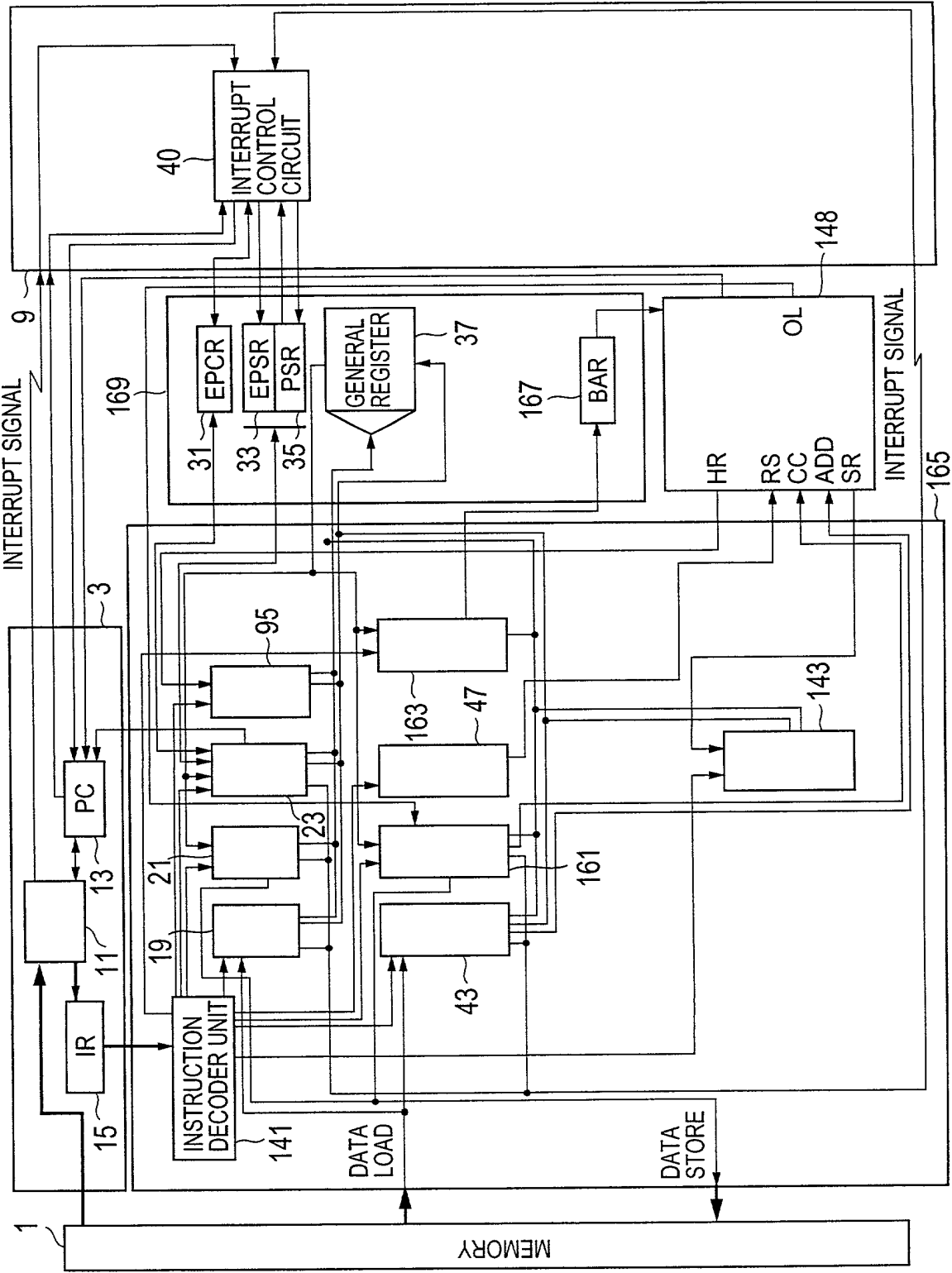


FIG. 32

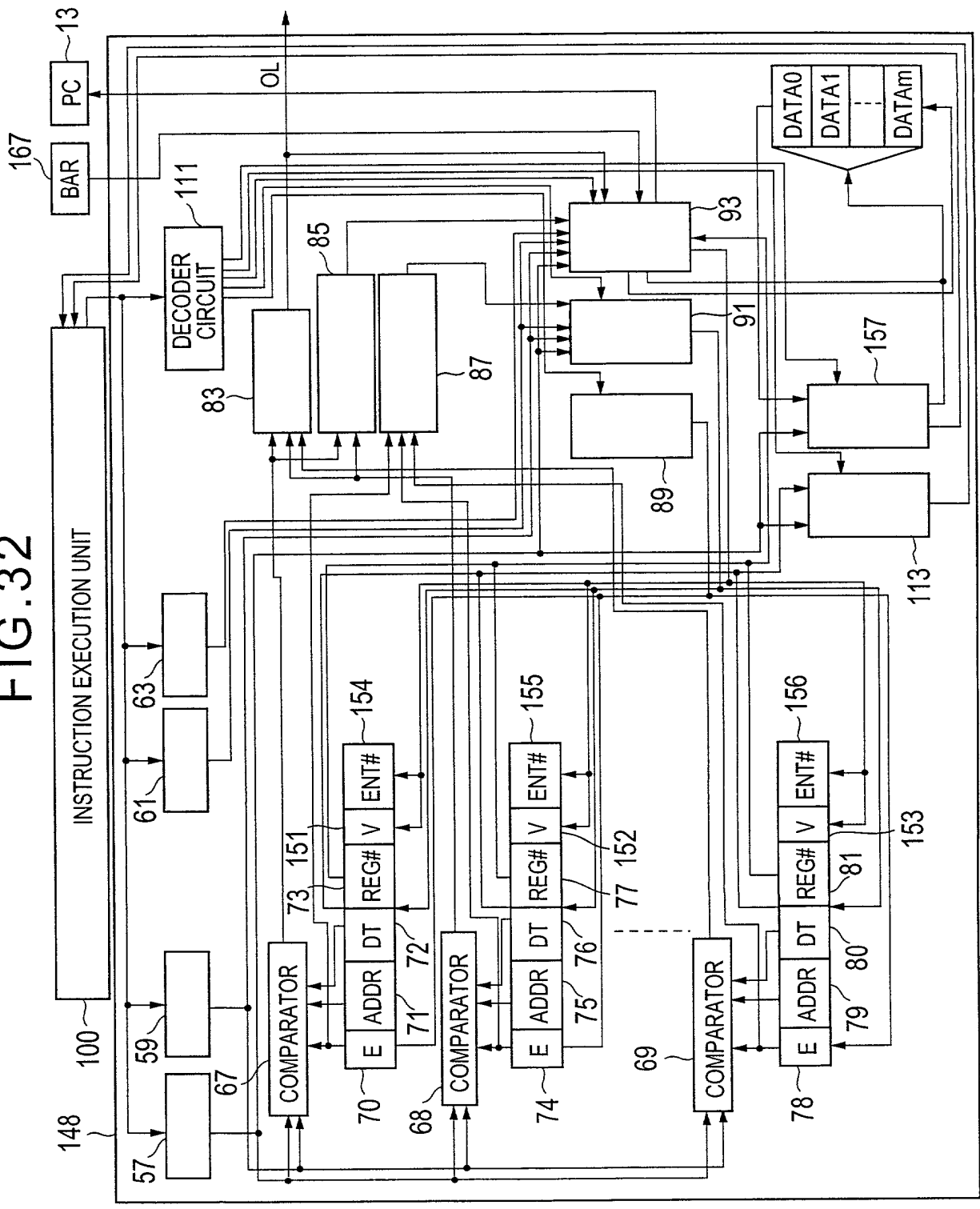


FIG. 33

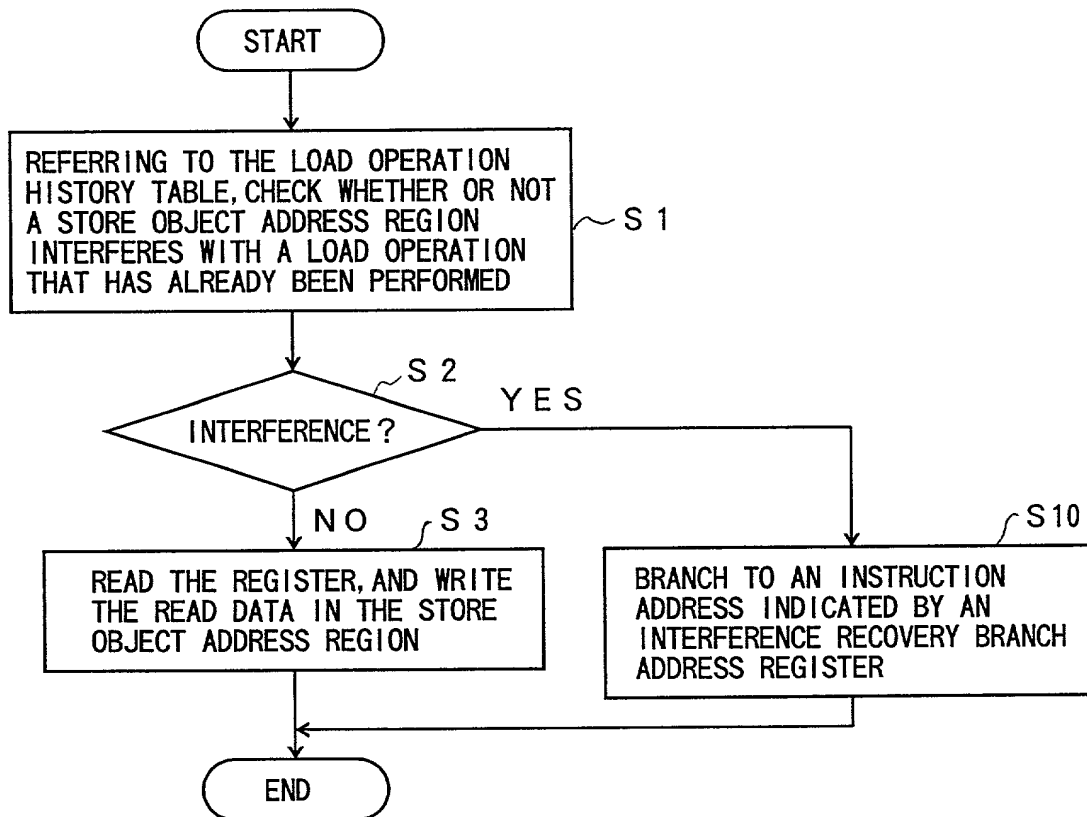


FIG. 34

OP-CODE	GR1	GR2	GRS
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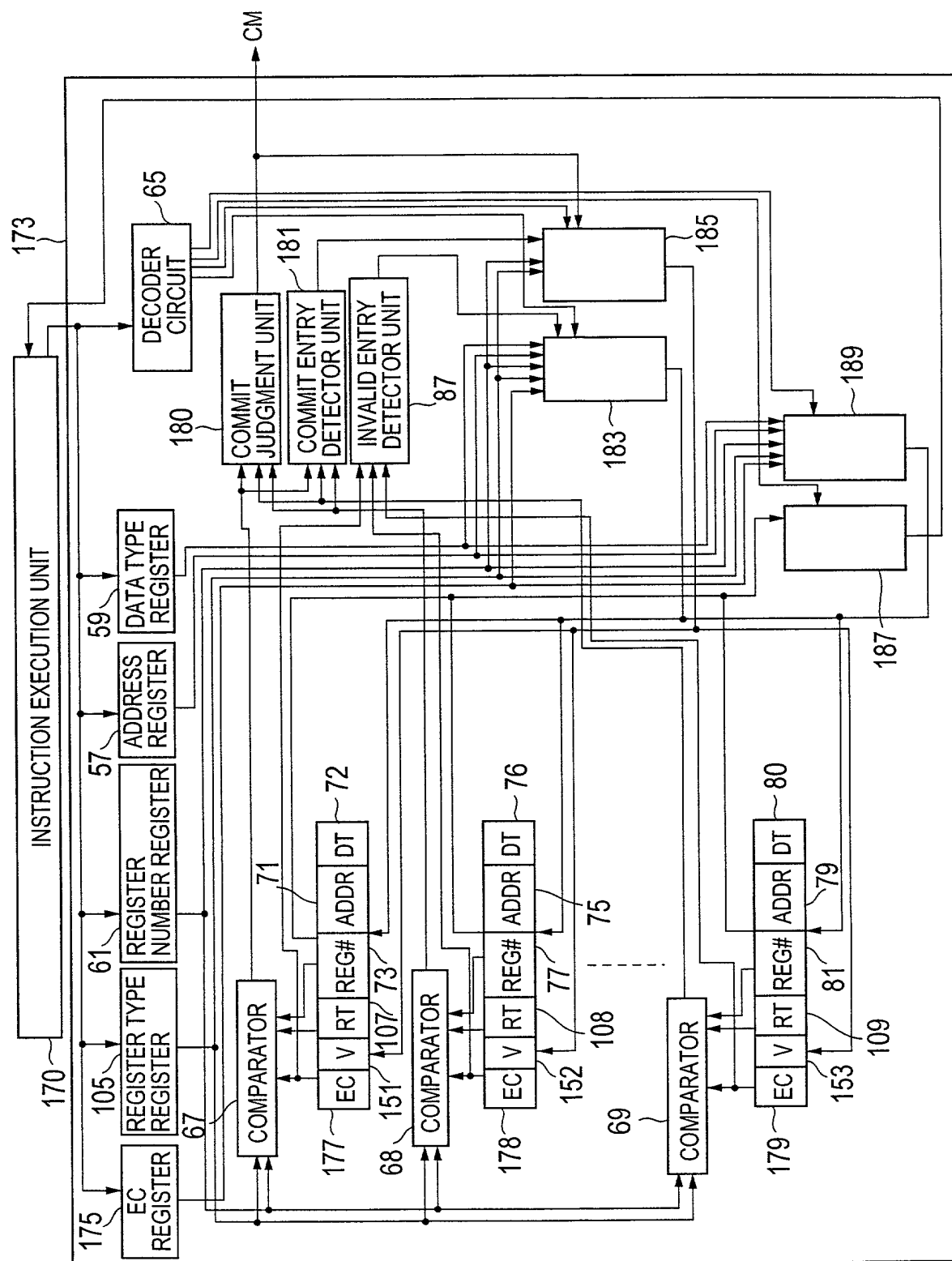


FIG. 37

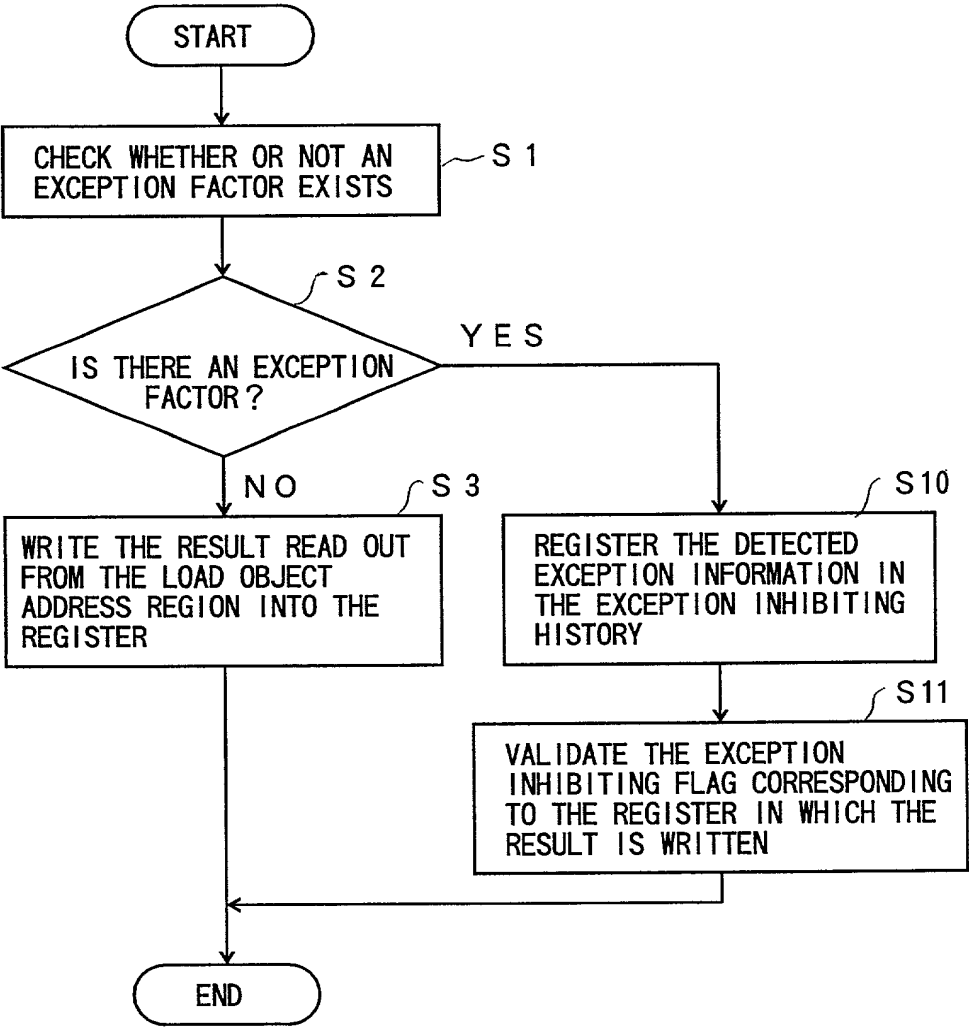


FIG. 38

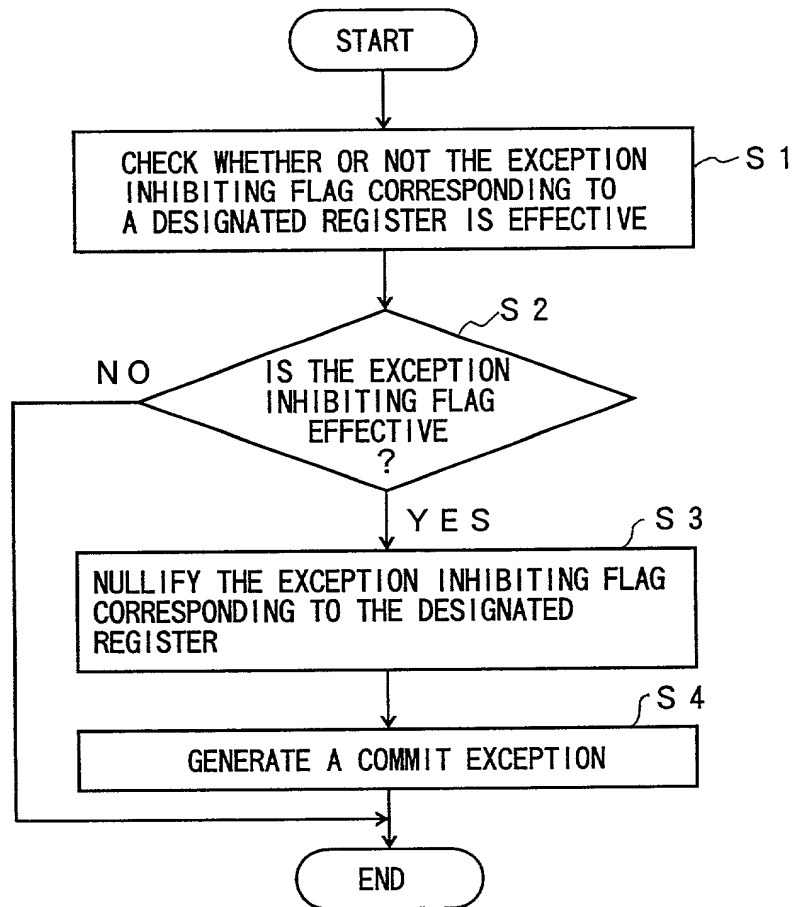


FIG. 39

OP-CODE	GR	
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FIG.40

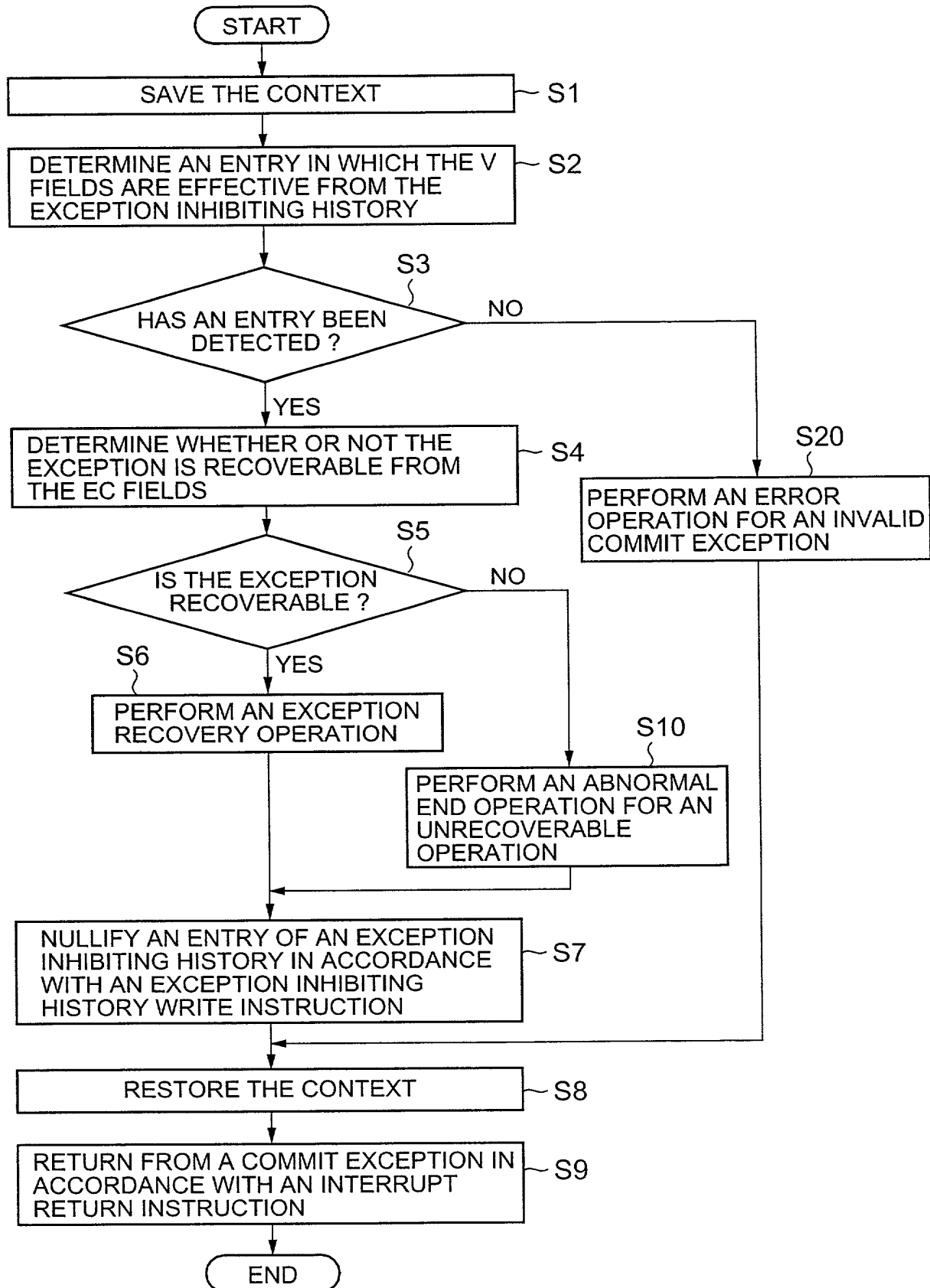


FIG. 41

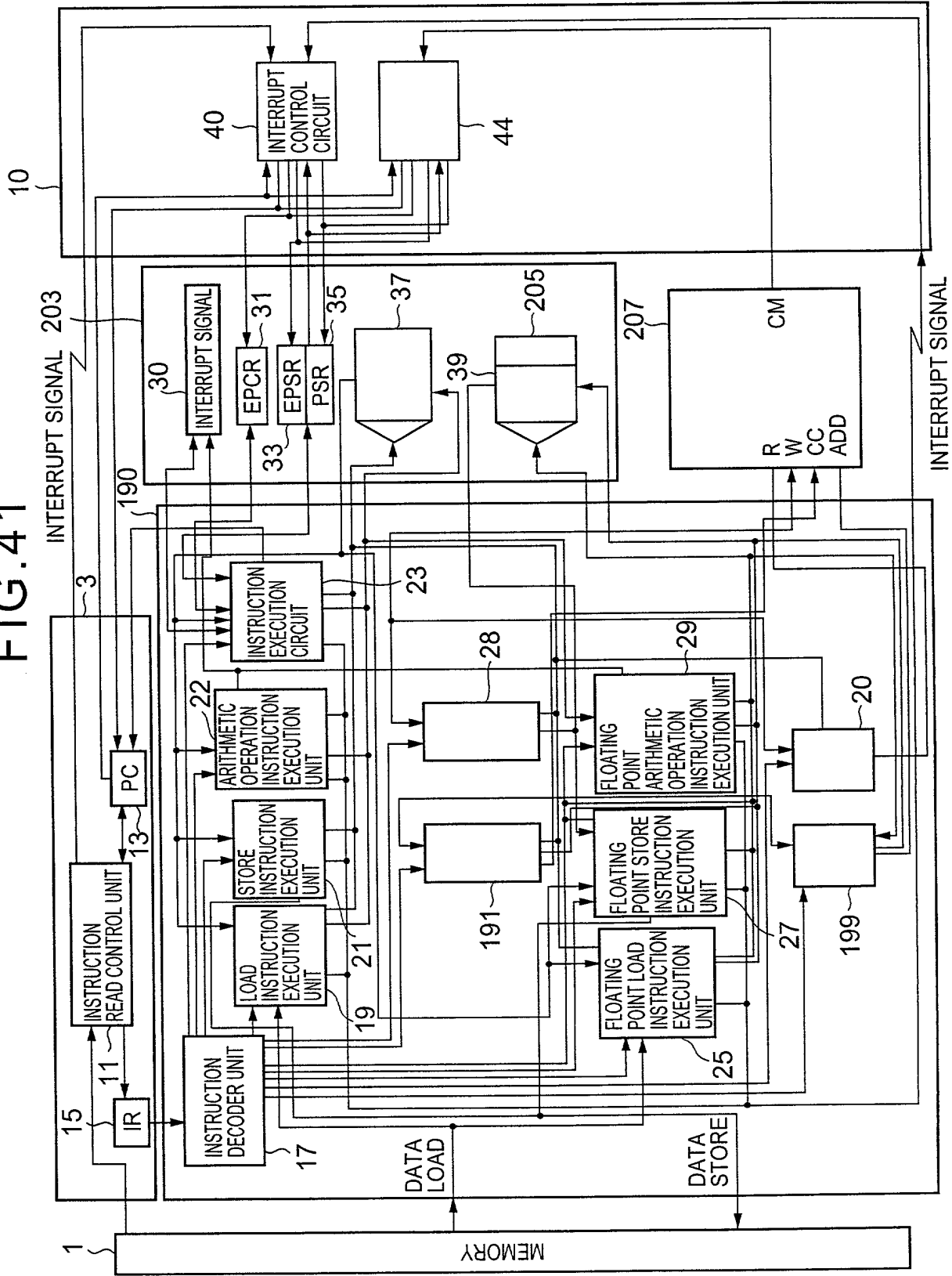


FIG. 42

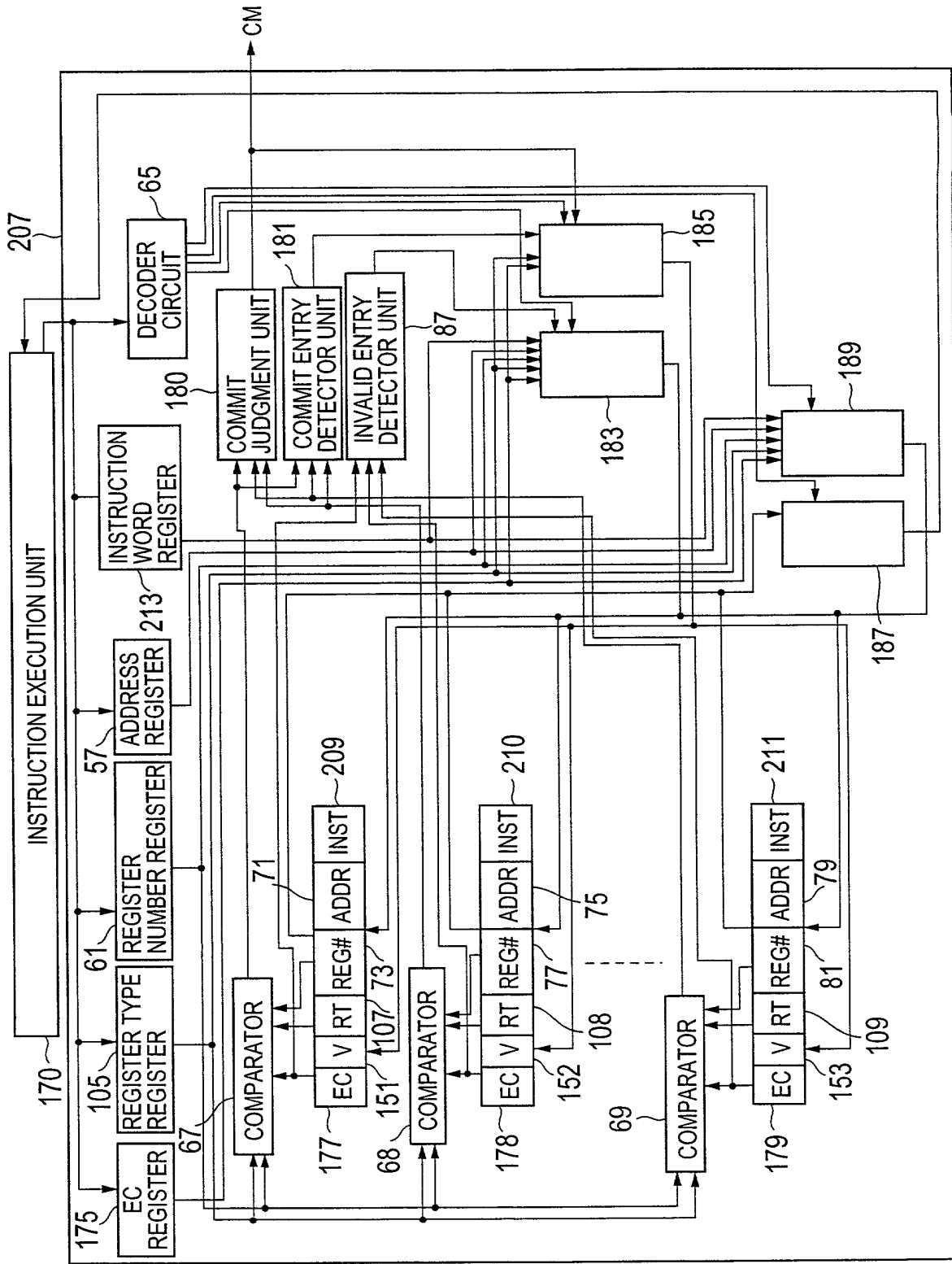


FIG. 43

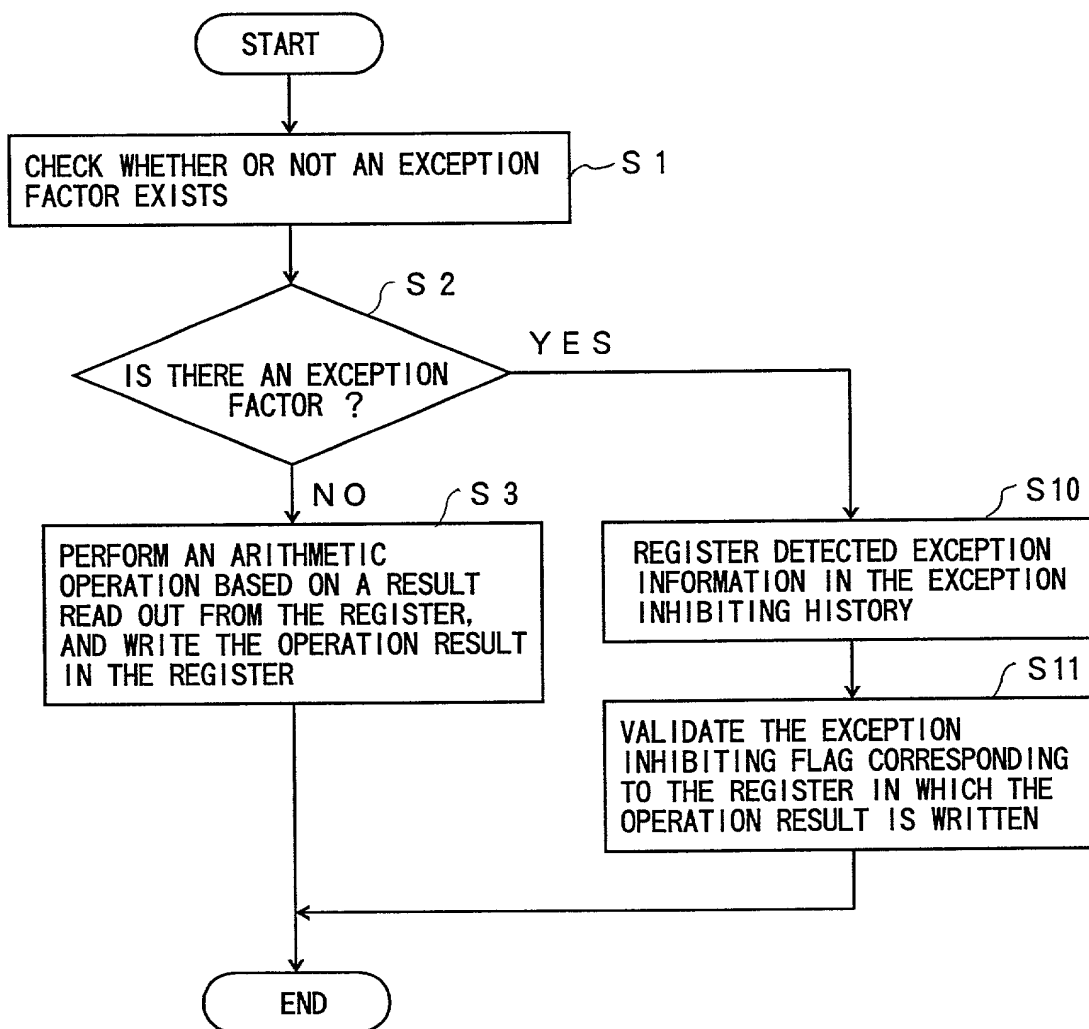


FIG. 44

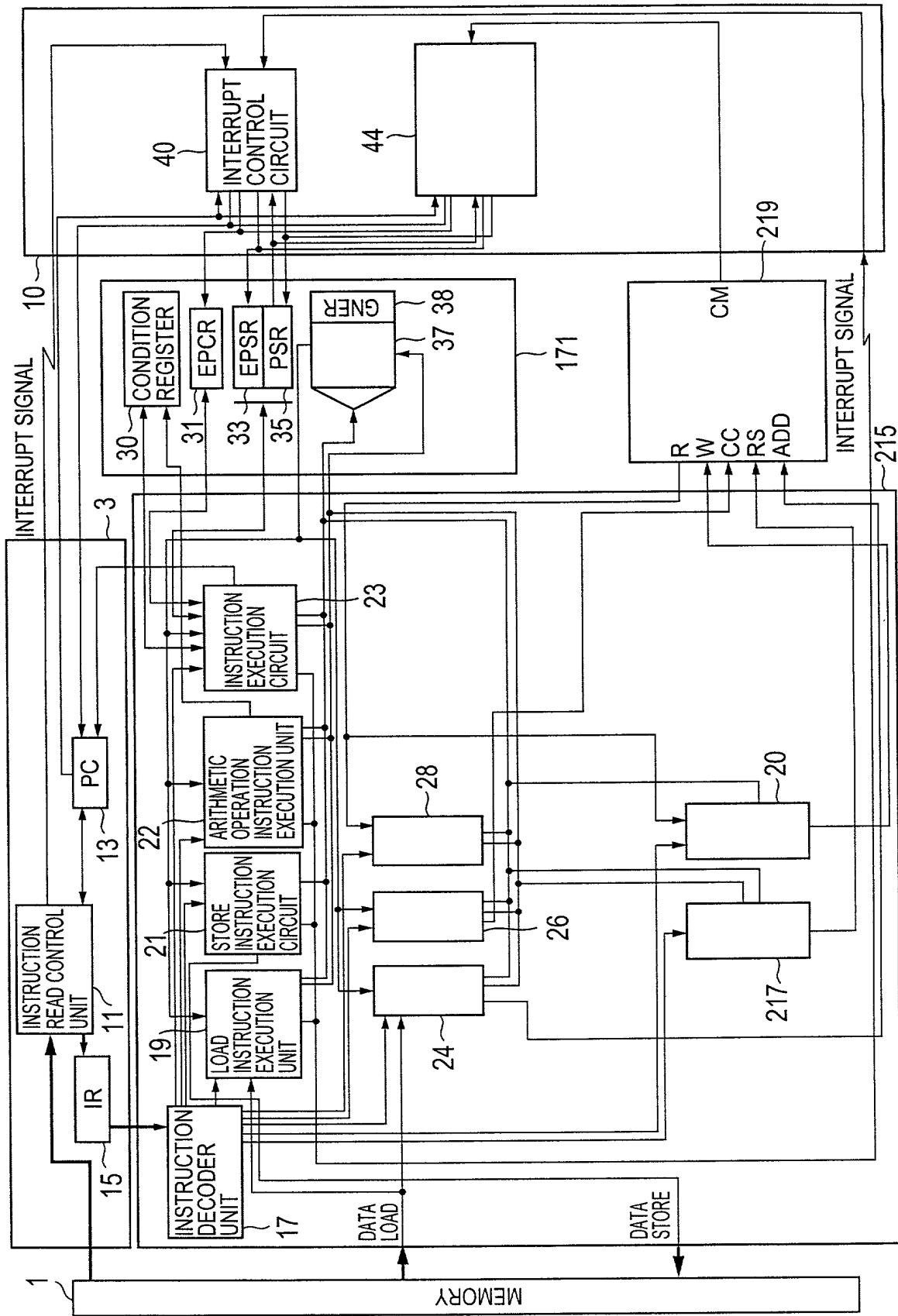


FIG. 45

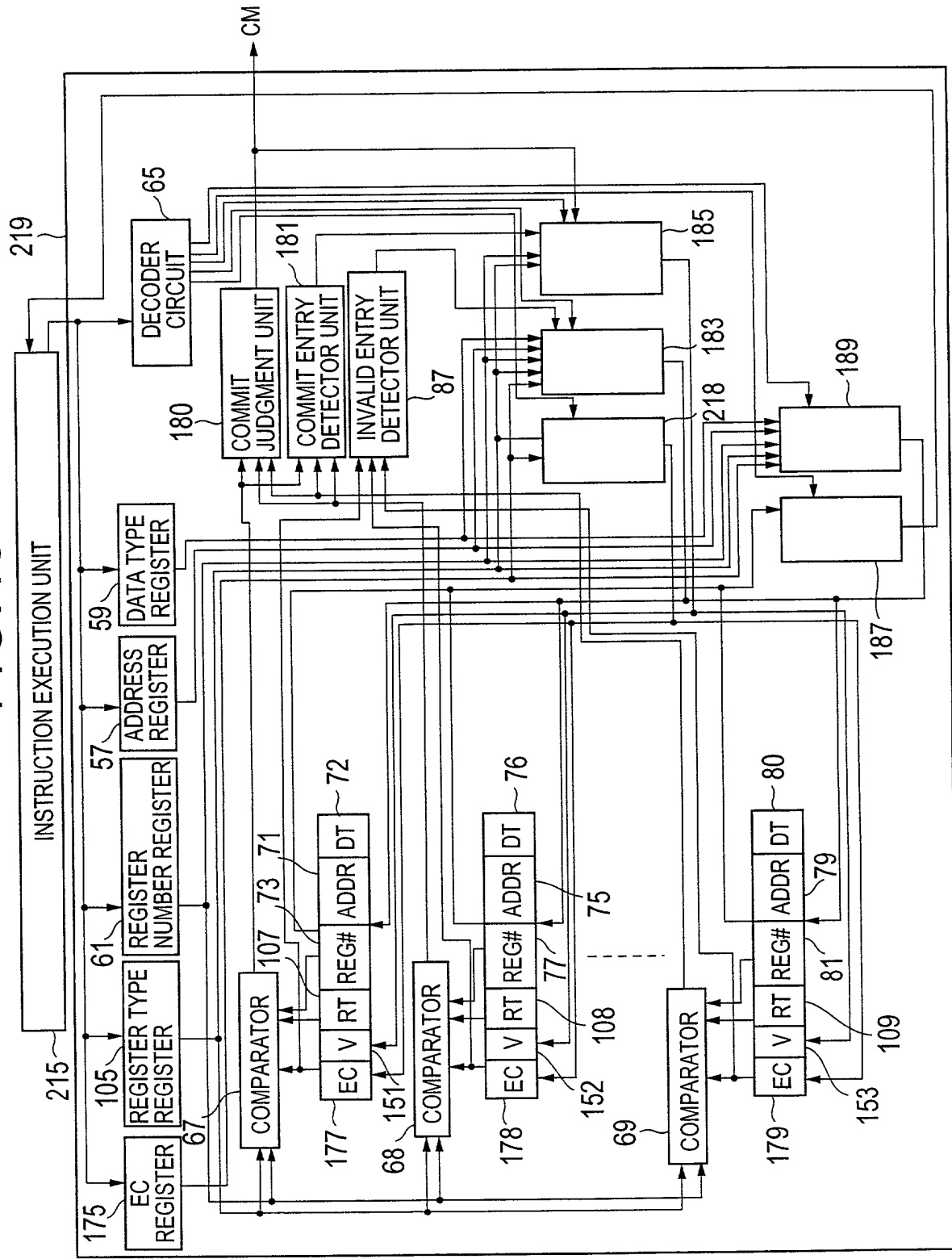


FIG. 46

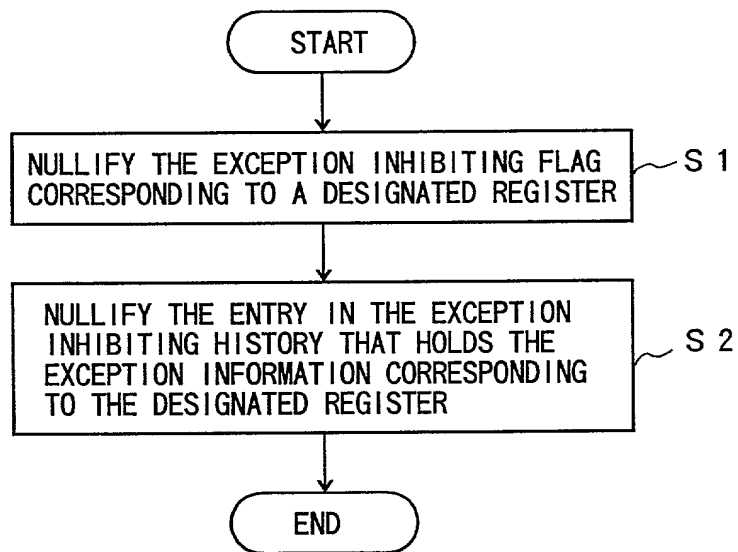


FIG. 47

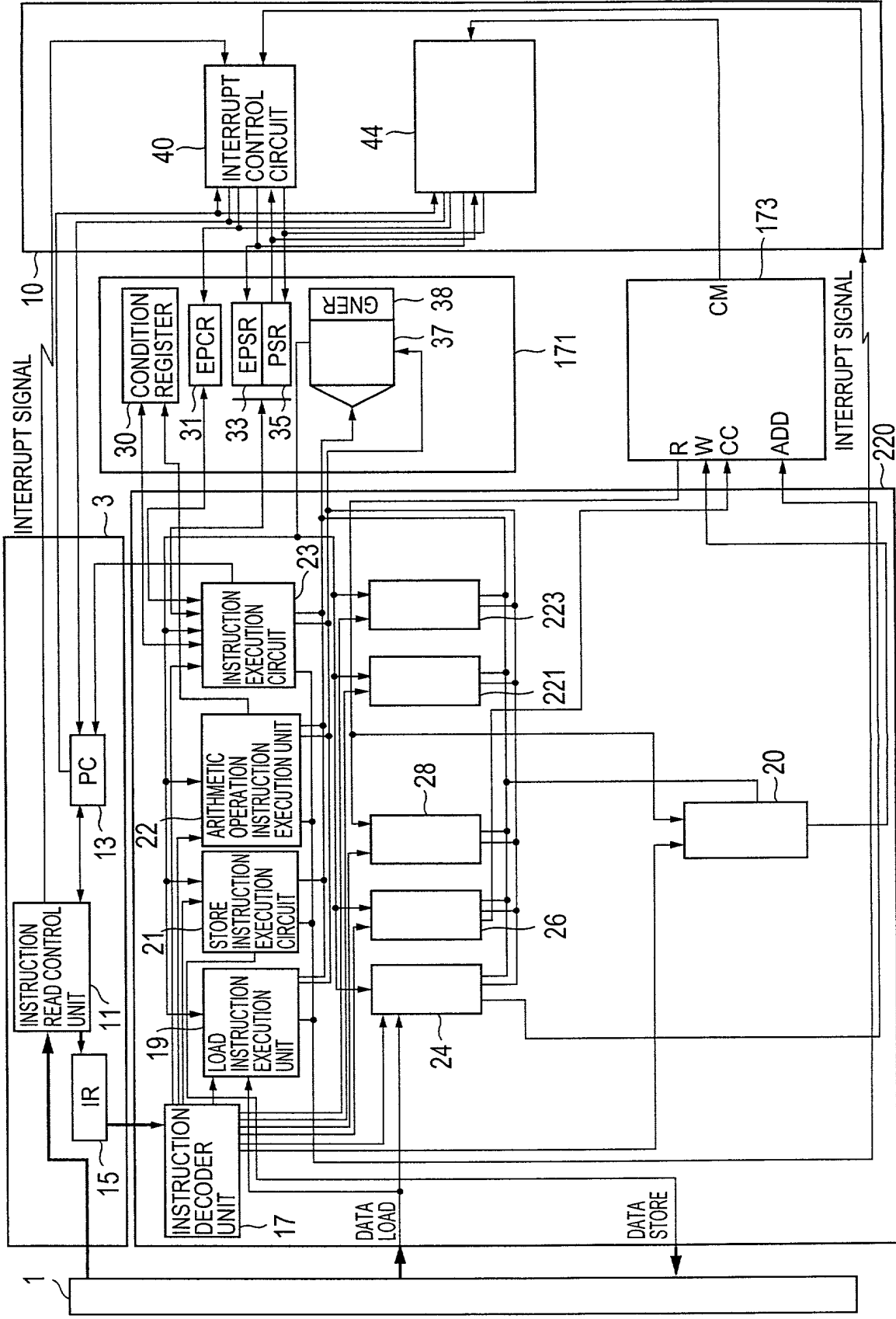


FIG. 48

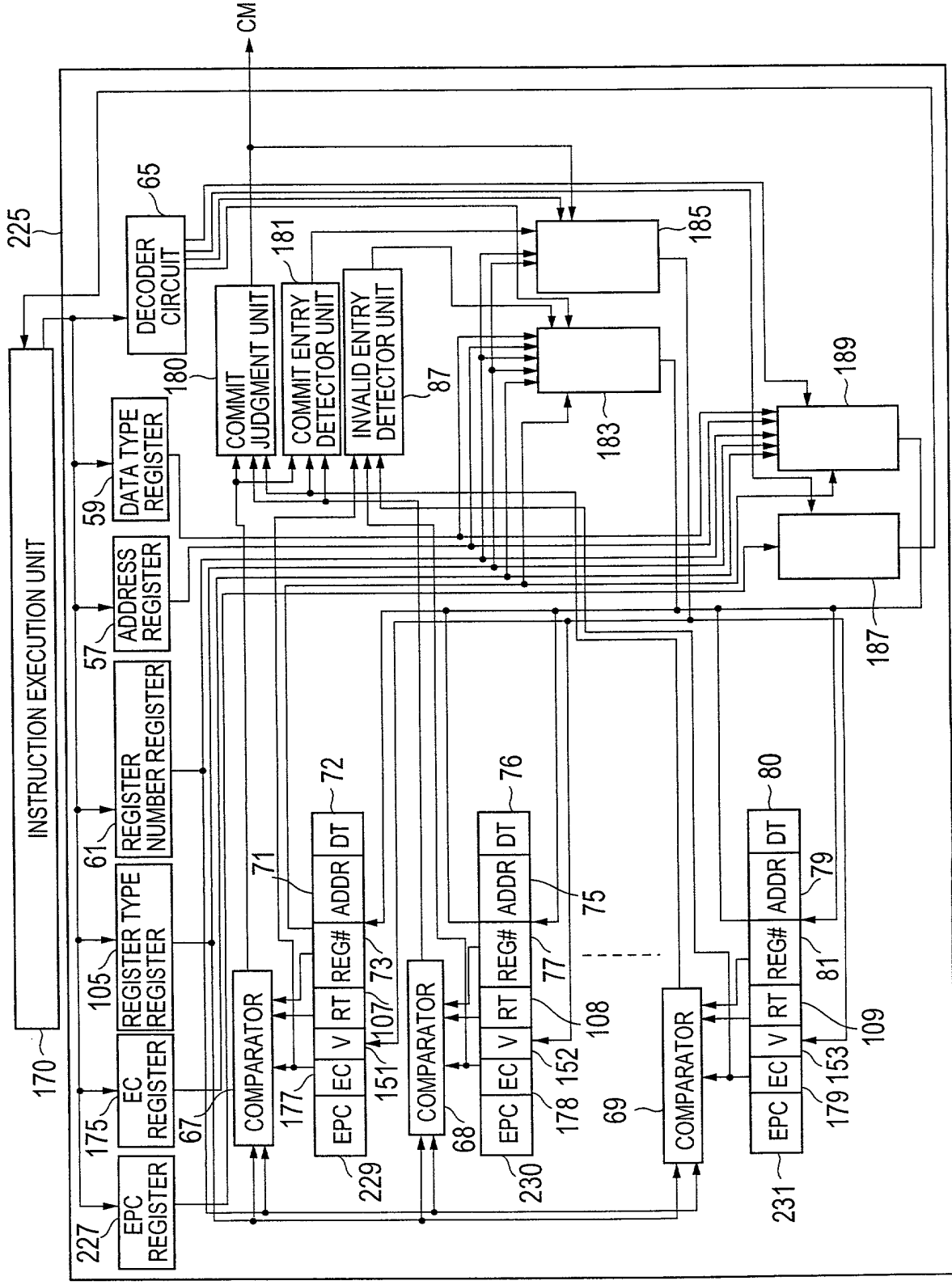


FIG.49

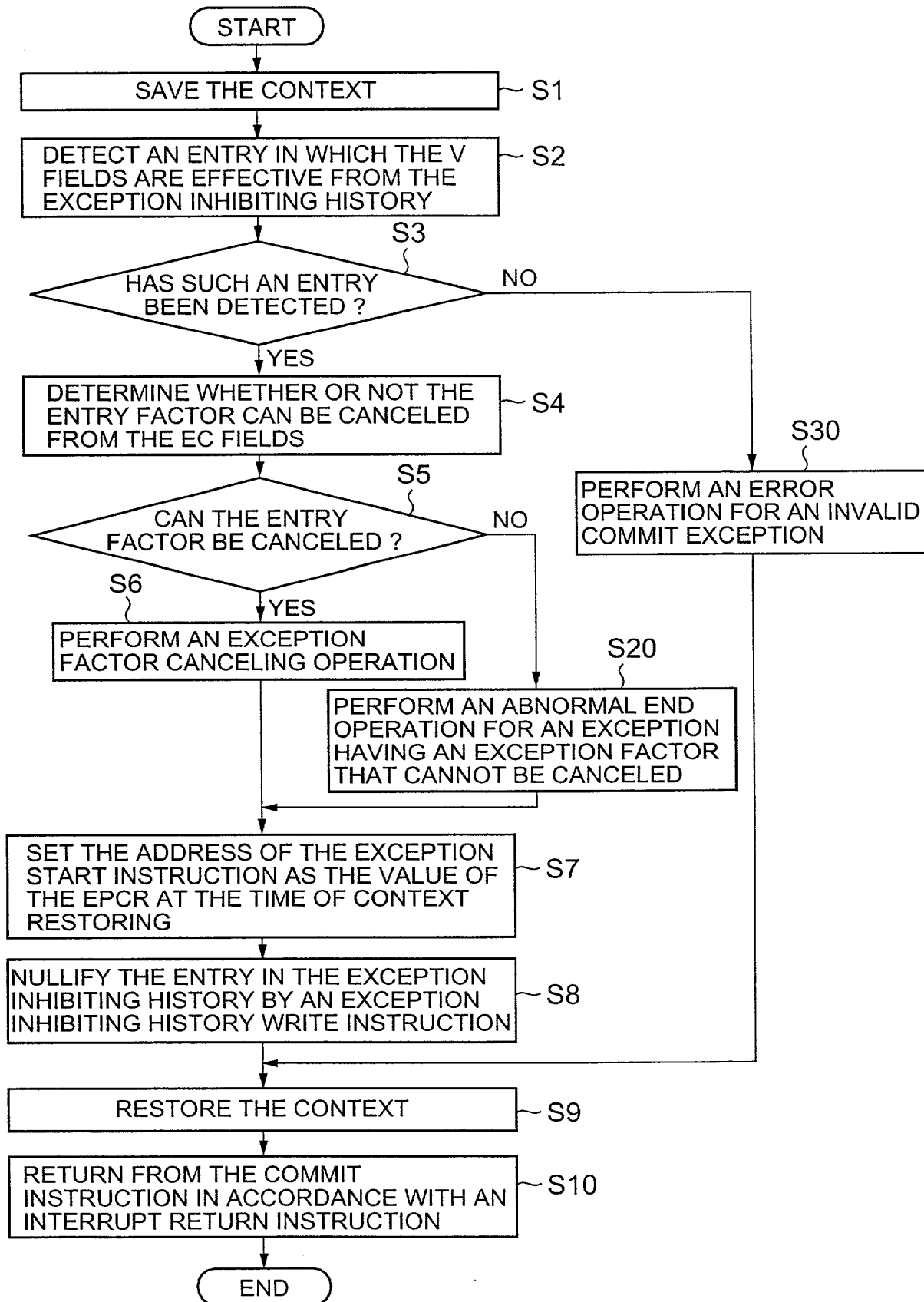


FIG.50

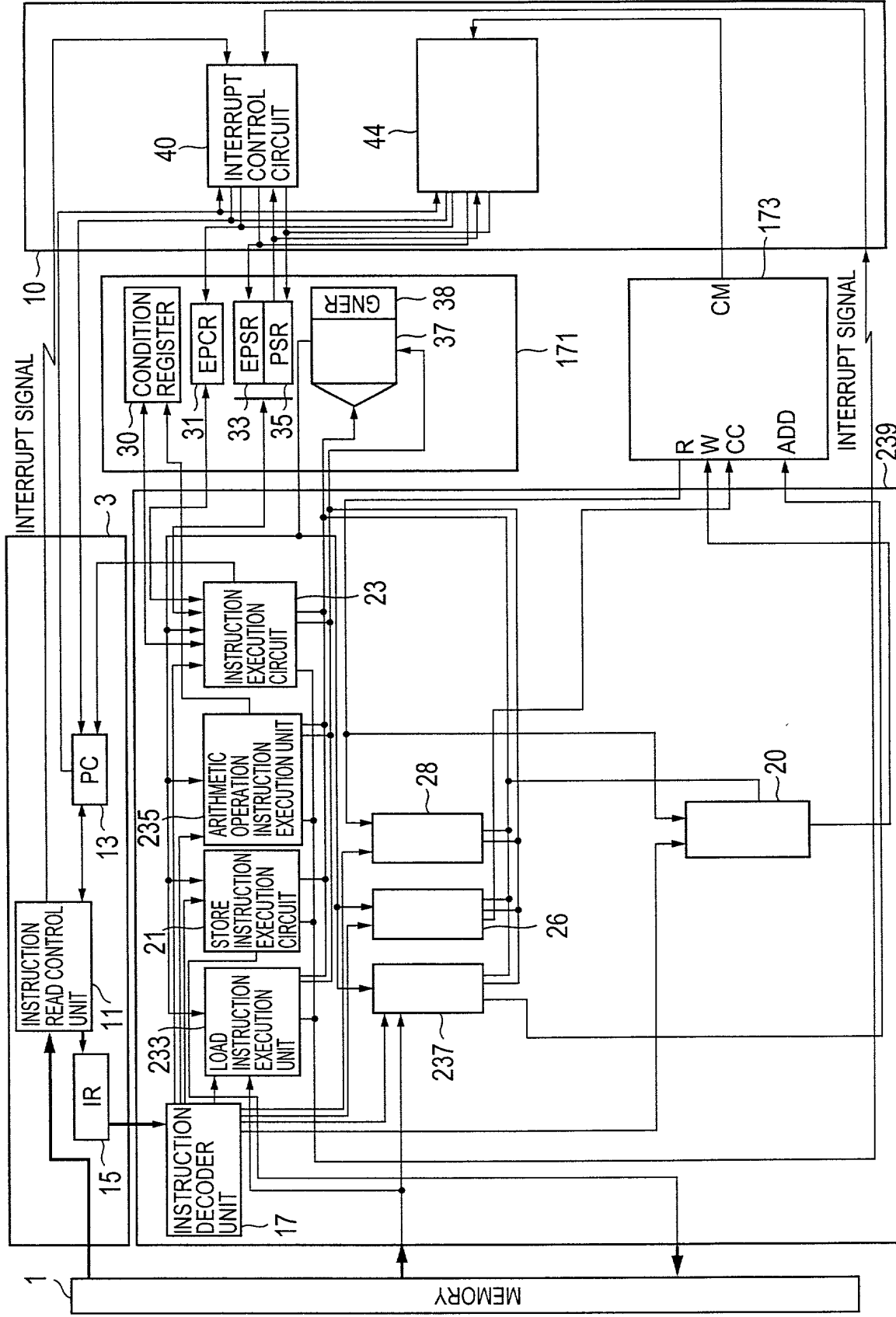


FIG. 51

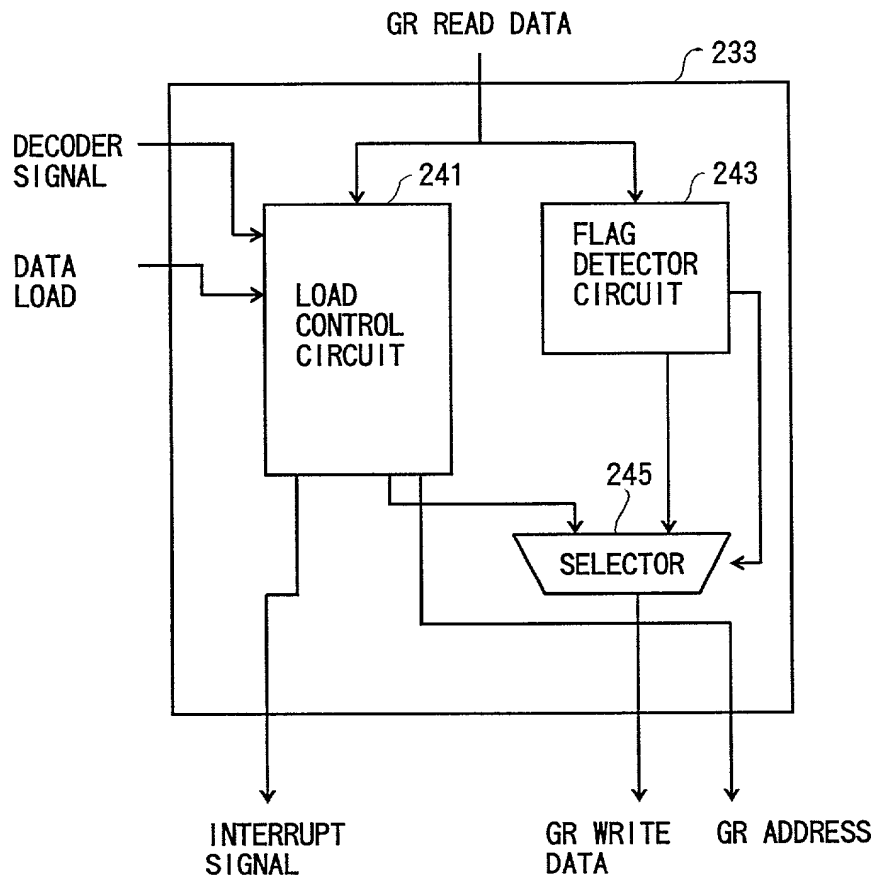


FIG. 52

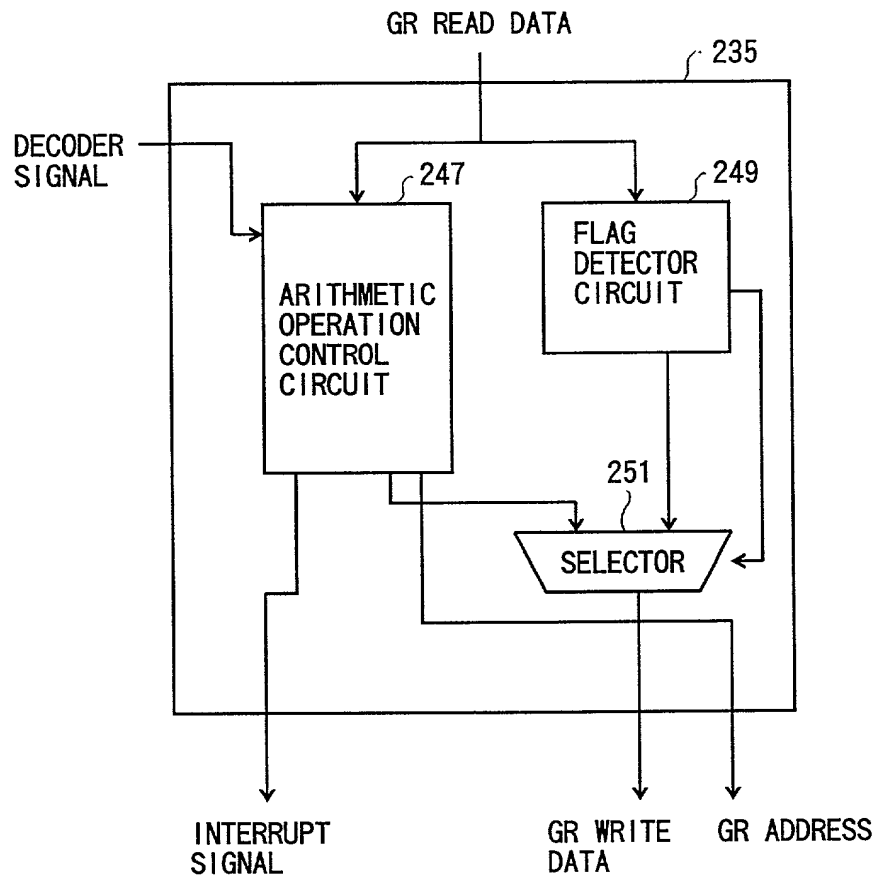


FIG. 53

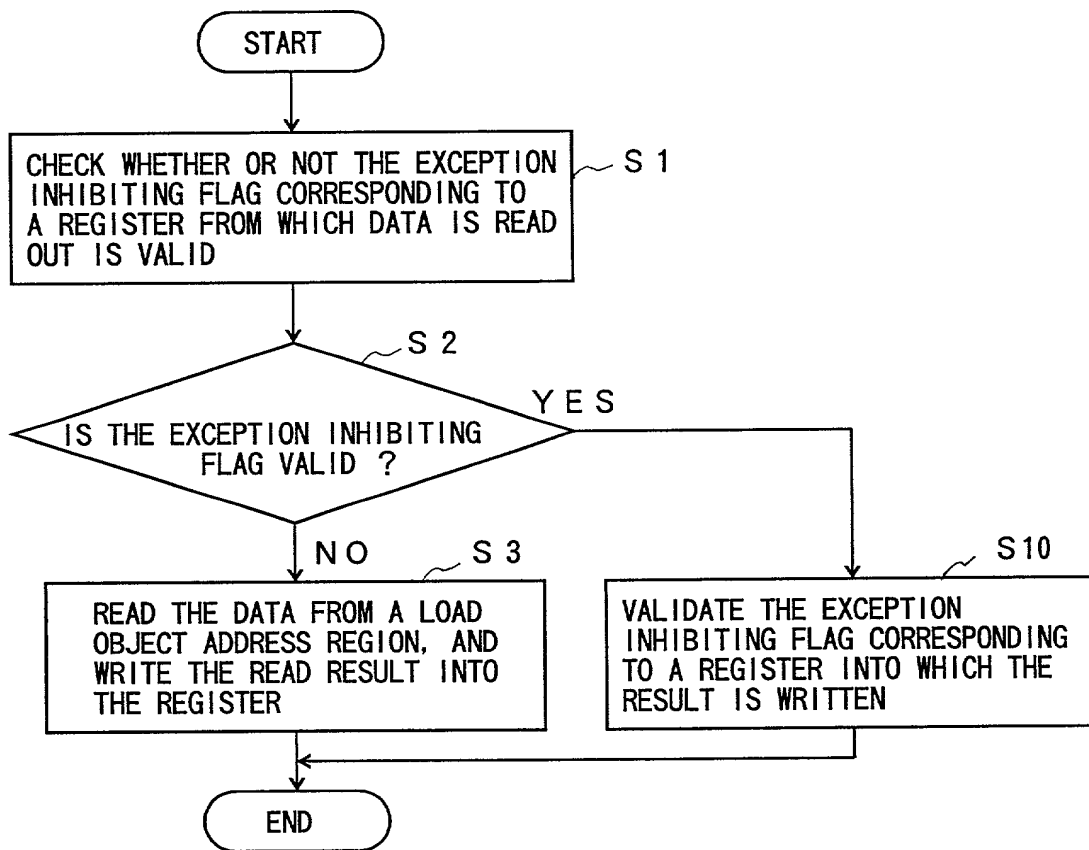


FIG. 54

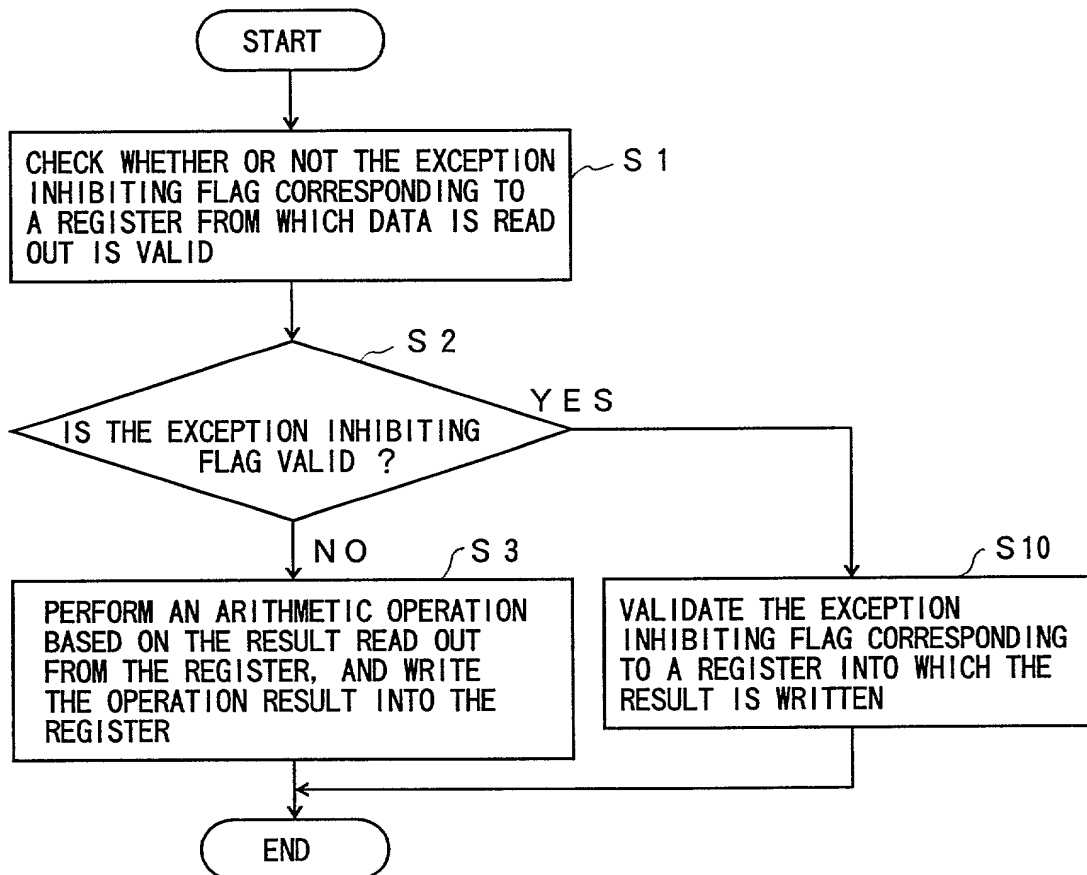


FIG.55

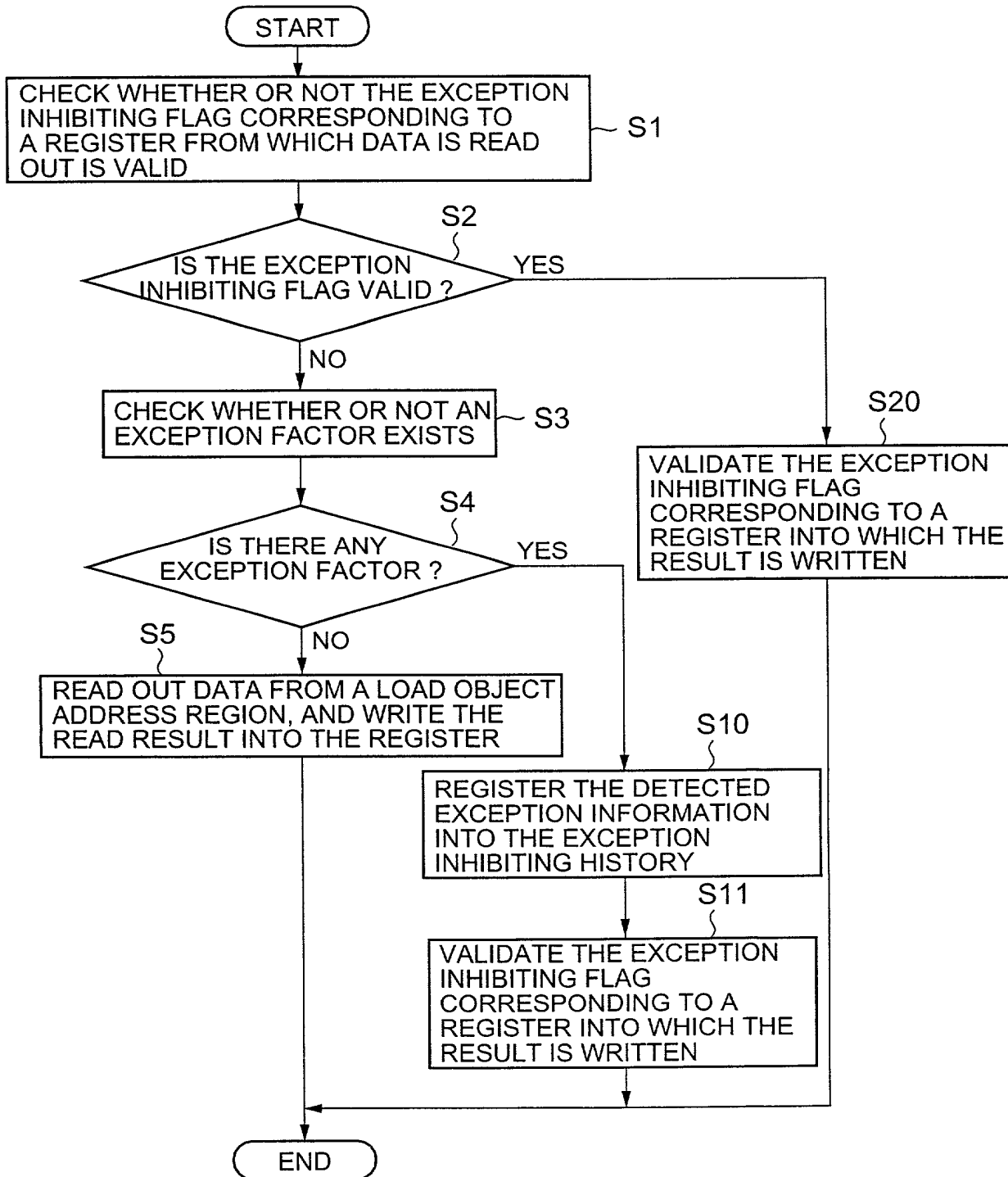


FIG. 56

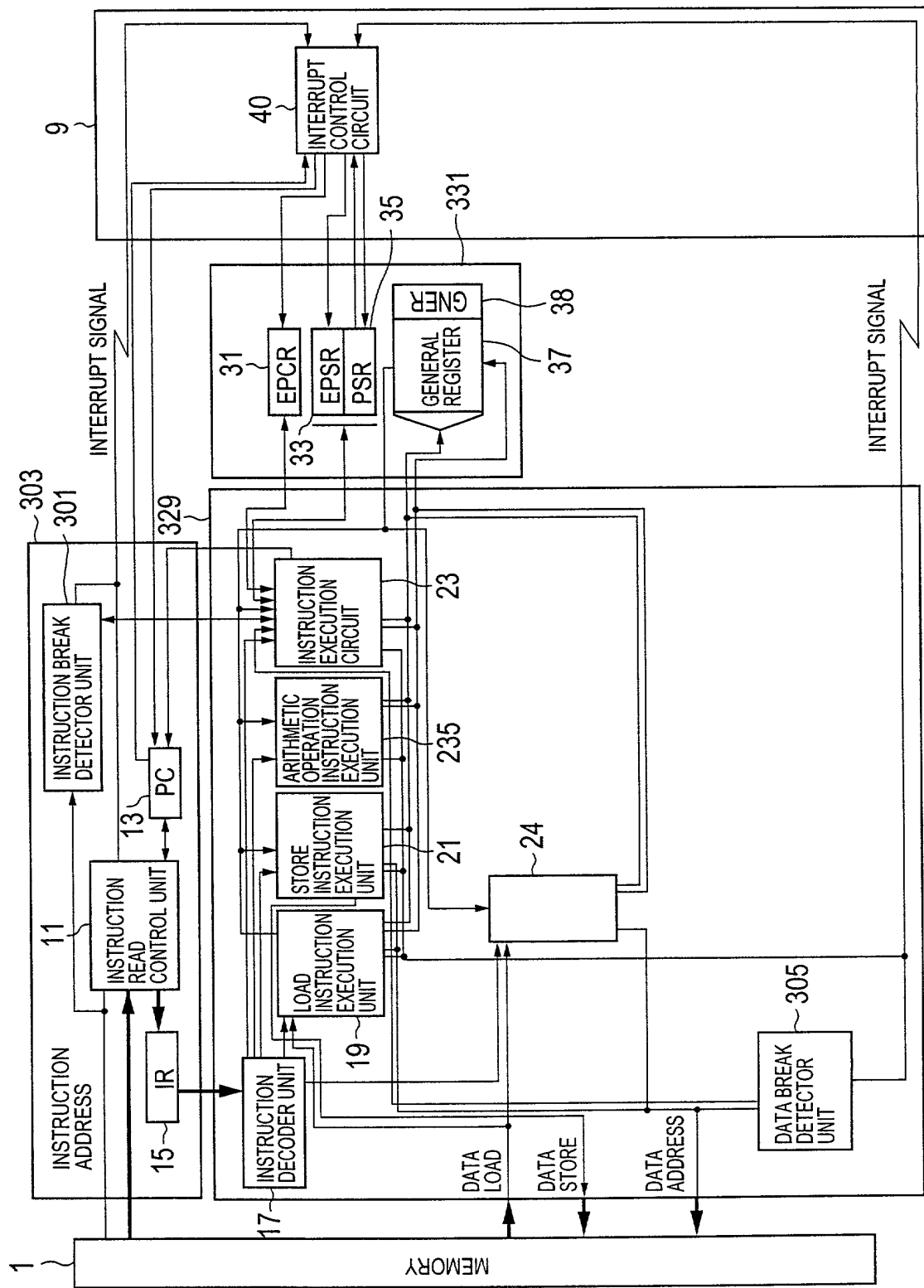


FIG.57

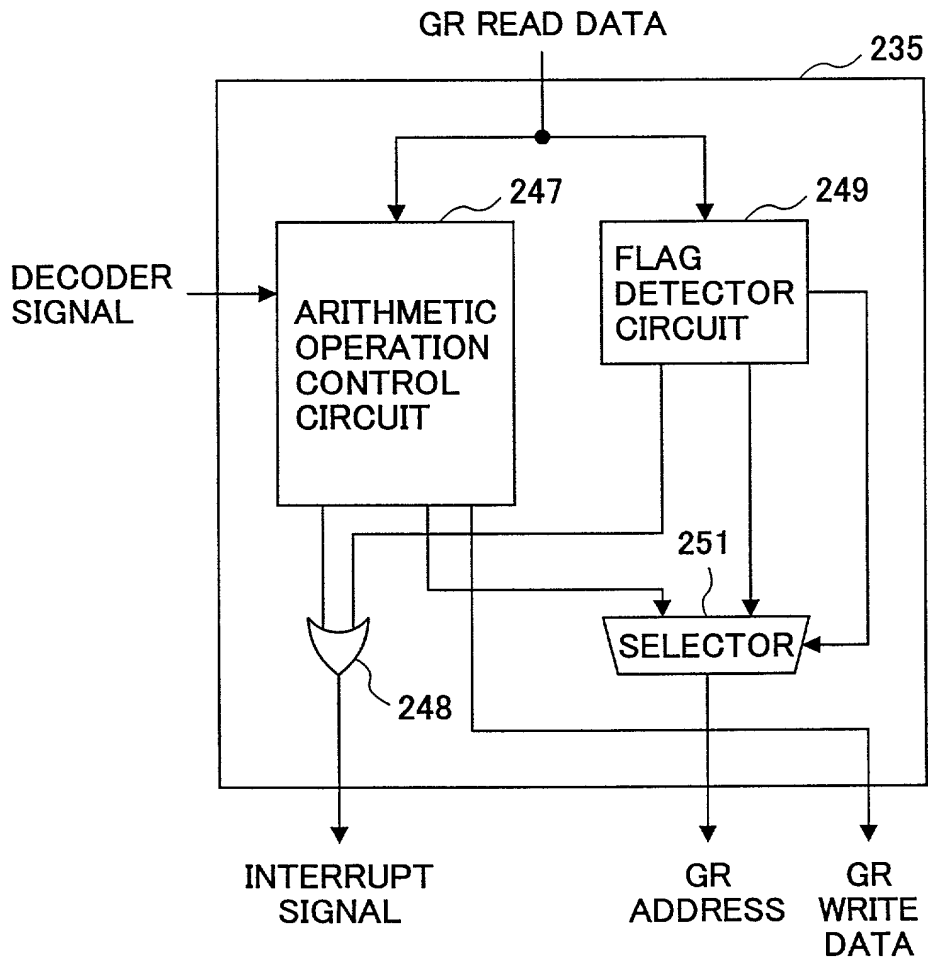


FIG.58

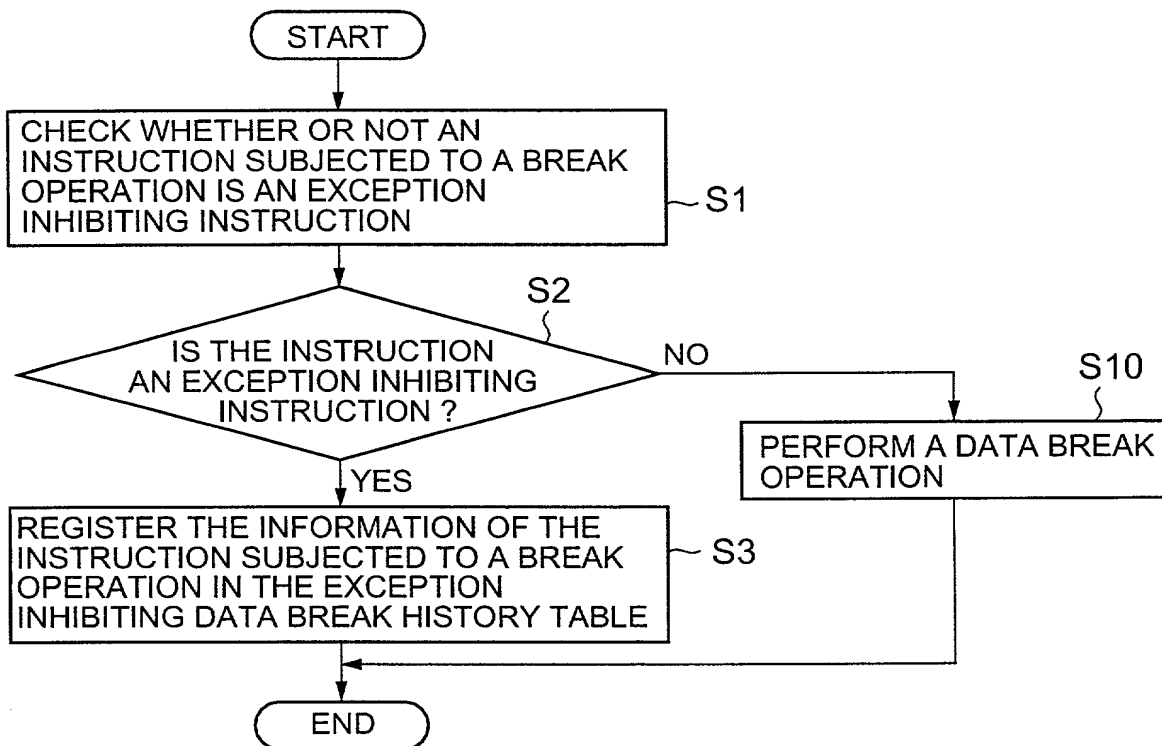


FIG.59

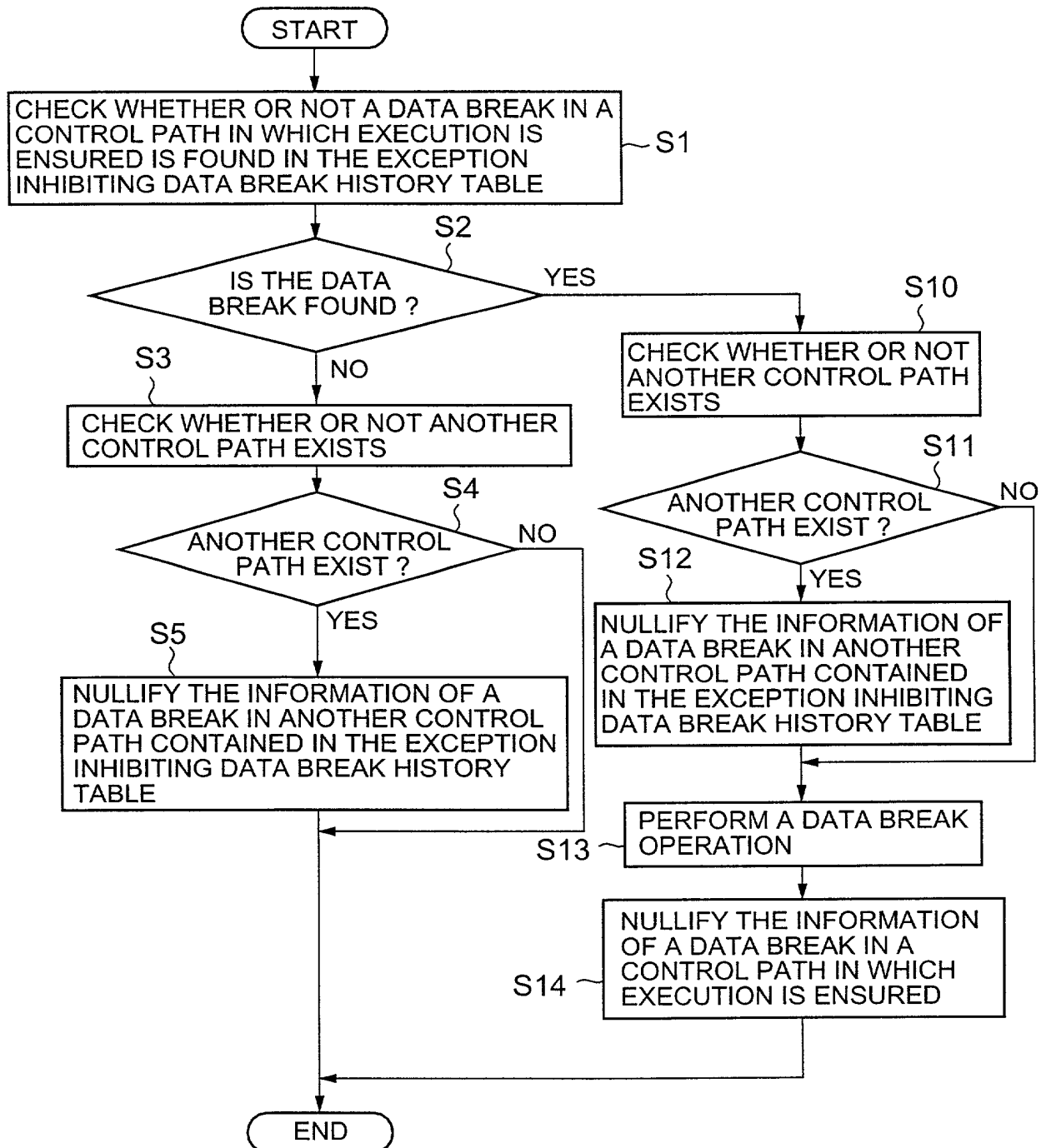


FIG.60

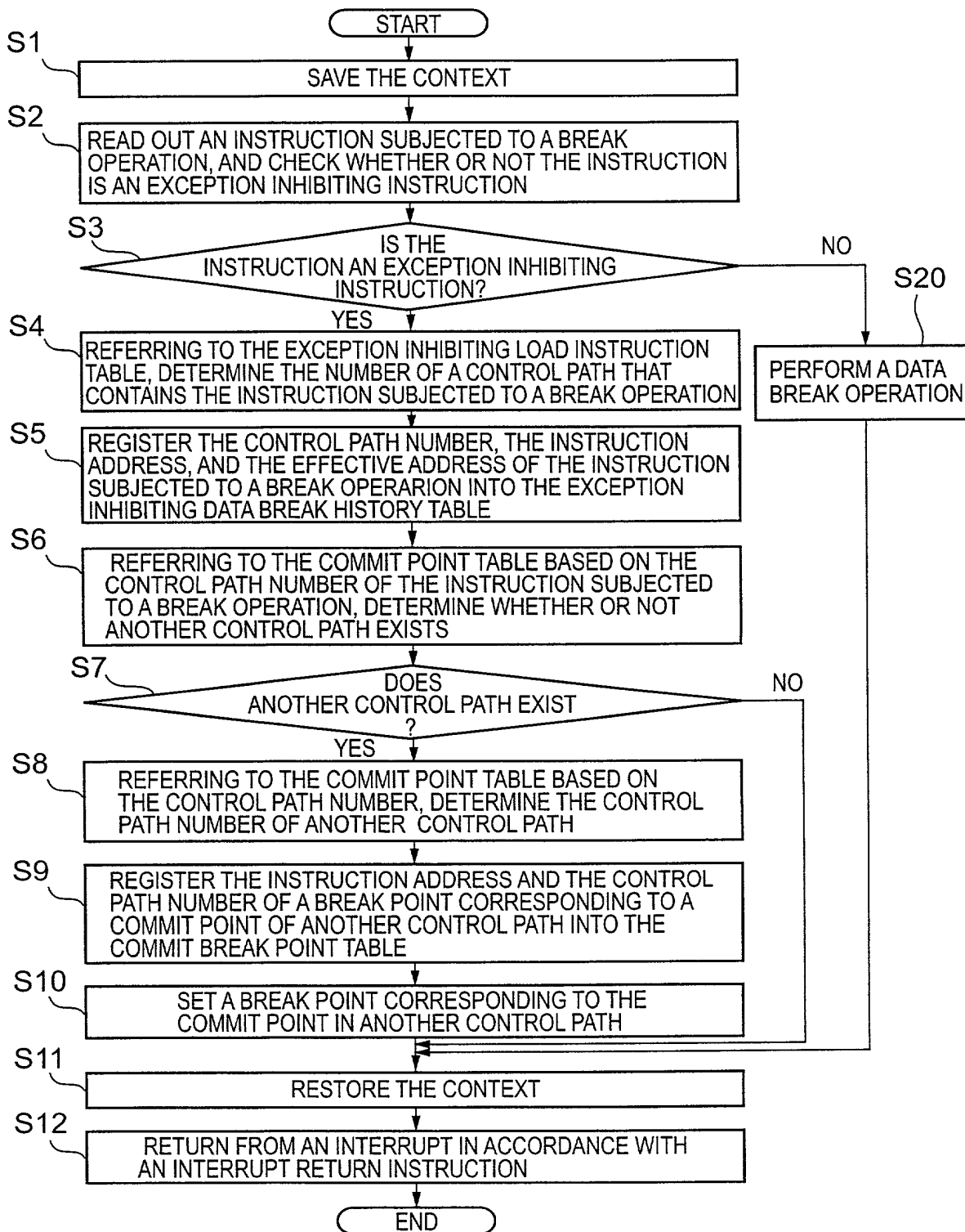


FIG.61

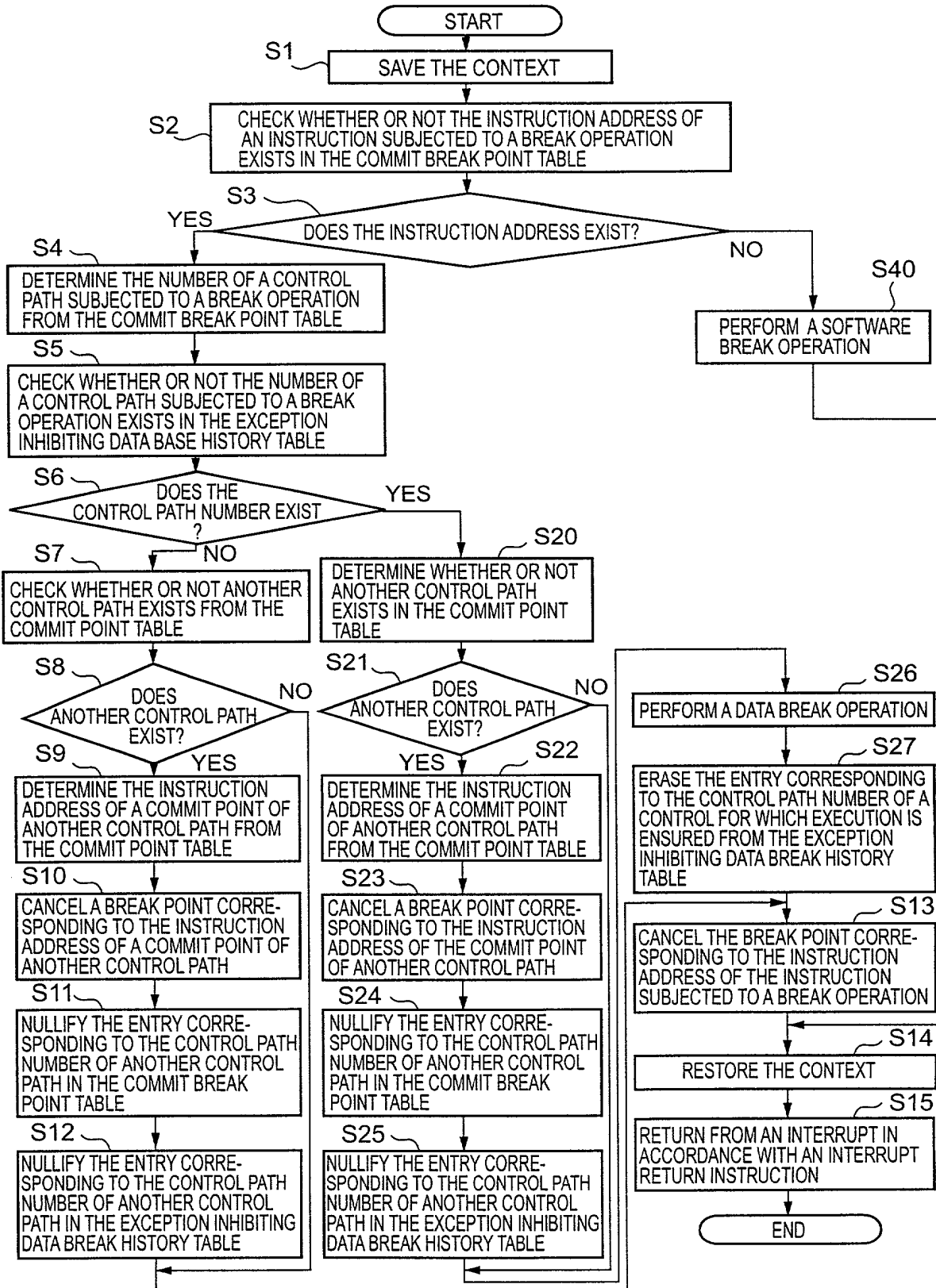


FIG.62

INSTRUCTION ADDRESS	PATH IDENTIFICATION NUMBER
a0	p0
a1	p1
:	:
:	:
ai	pi

FIG.63

PATH IDENTIFICATION NUMBER	INSTRUCTION ADDRESS	ANOTHER PATH IDENTIFICATION NUMBER
p0	b0	sp0
p1	b1	sp1
:	:	:
:	:	:
pj	bj	spj

FIG.64

INSTRUCTION ADDRESS	PATH IDENTIFICATION NUMBER
b0	p0
b1	p1
:	:
:	:
bk	pk

FIG.65

PATH IDENTIFICATION NUMBER	INSTRUCTION ADDRESS	EFFECTIVE ADDRESS
p0	c0	ec0
p1	c1	ec1
:	:	:
:	:	:
pl	cl	ec1

FIG.66

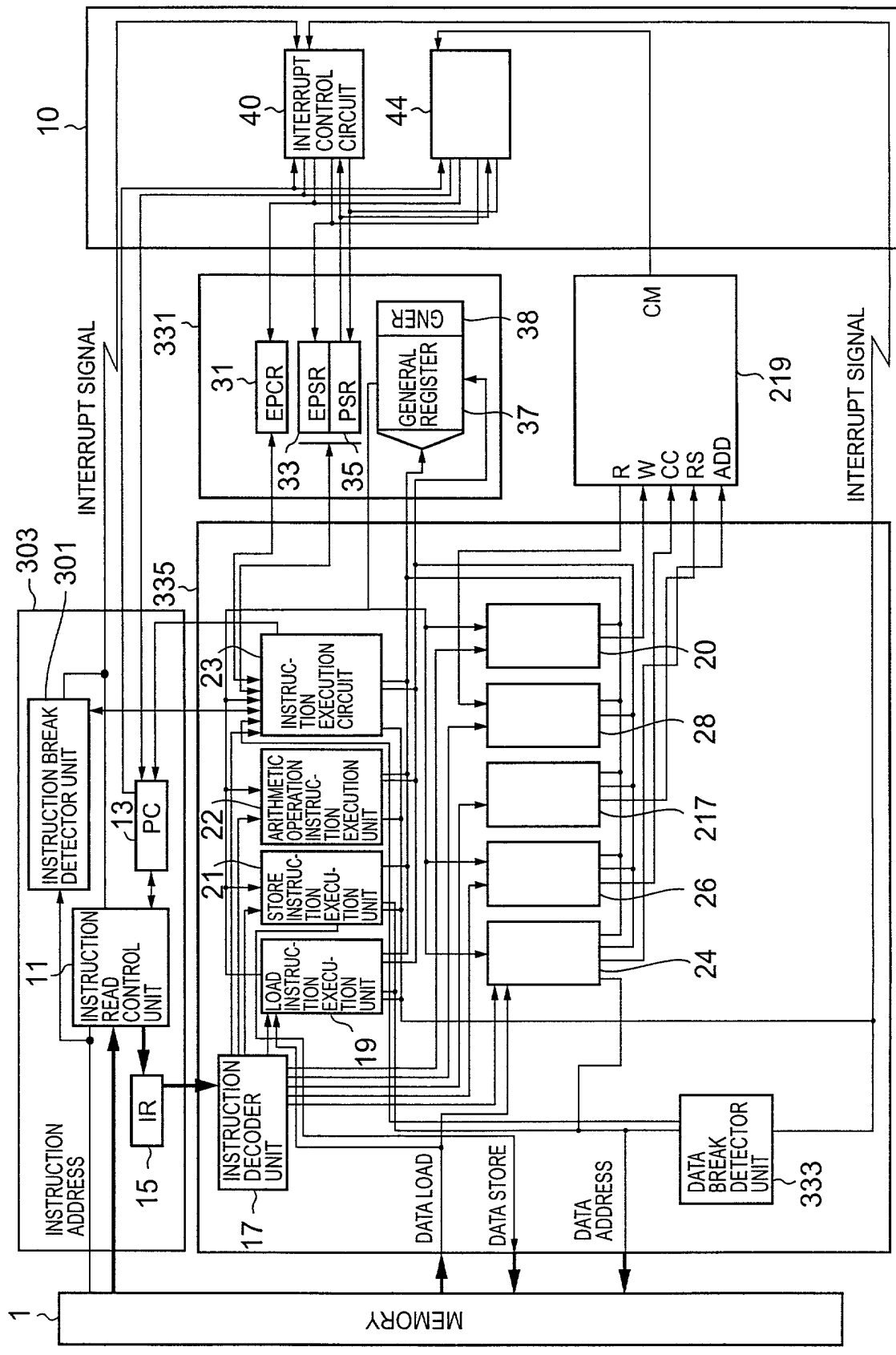


FIG.67

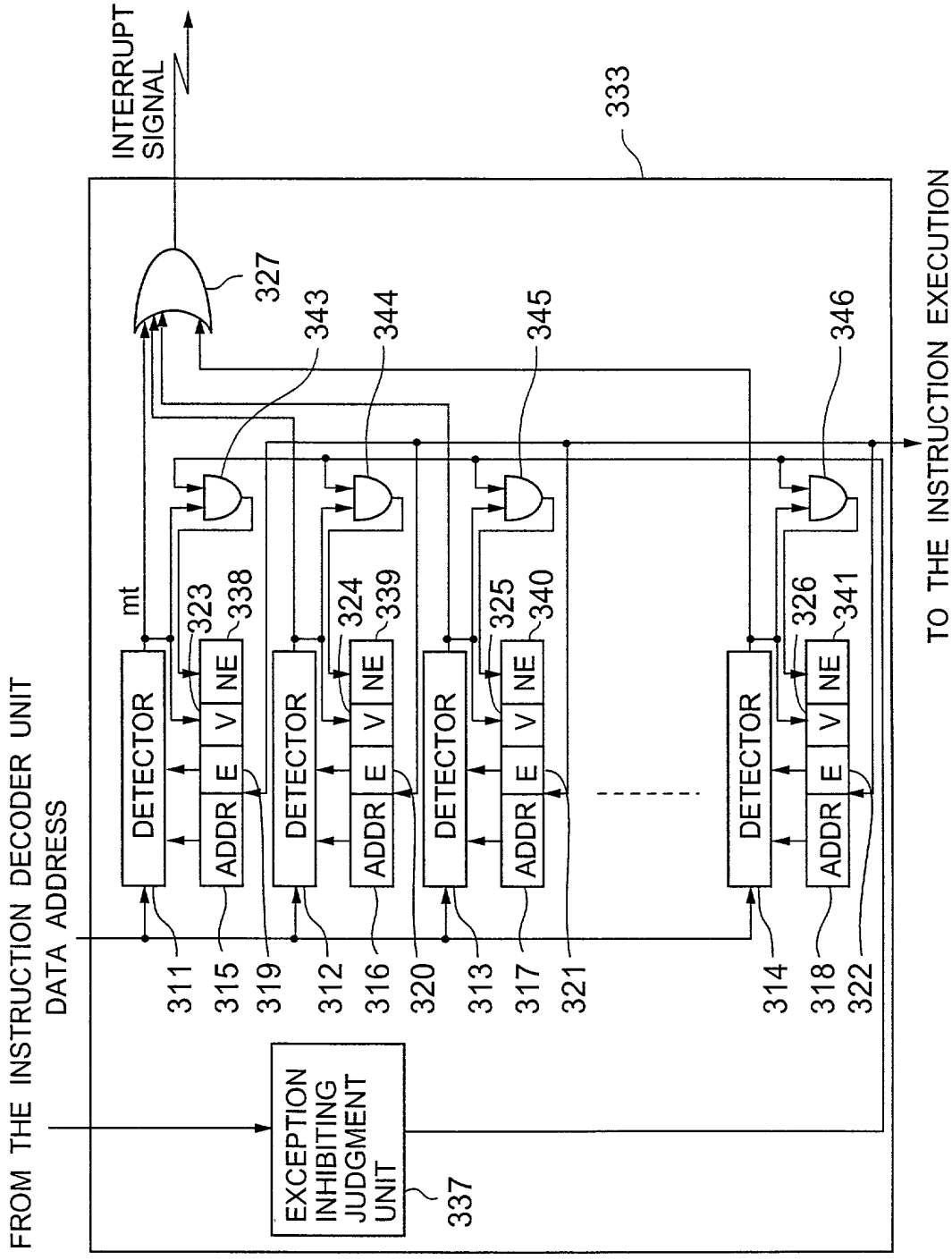


FIG. 68

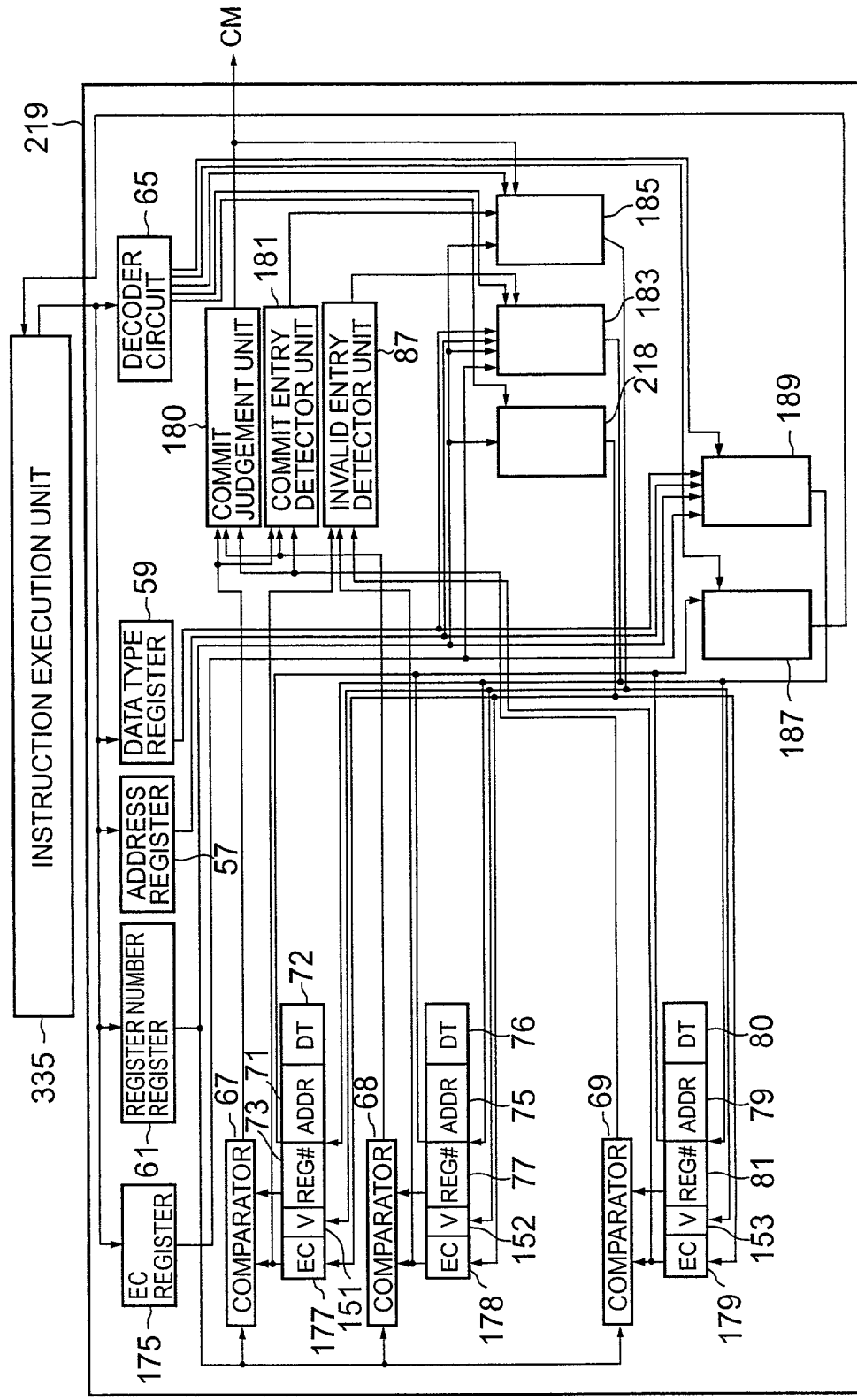
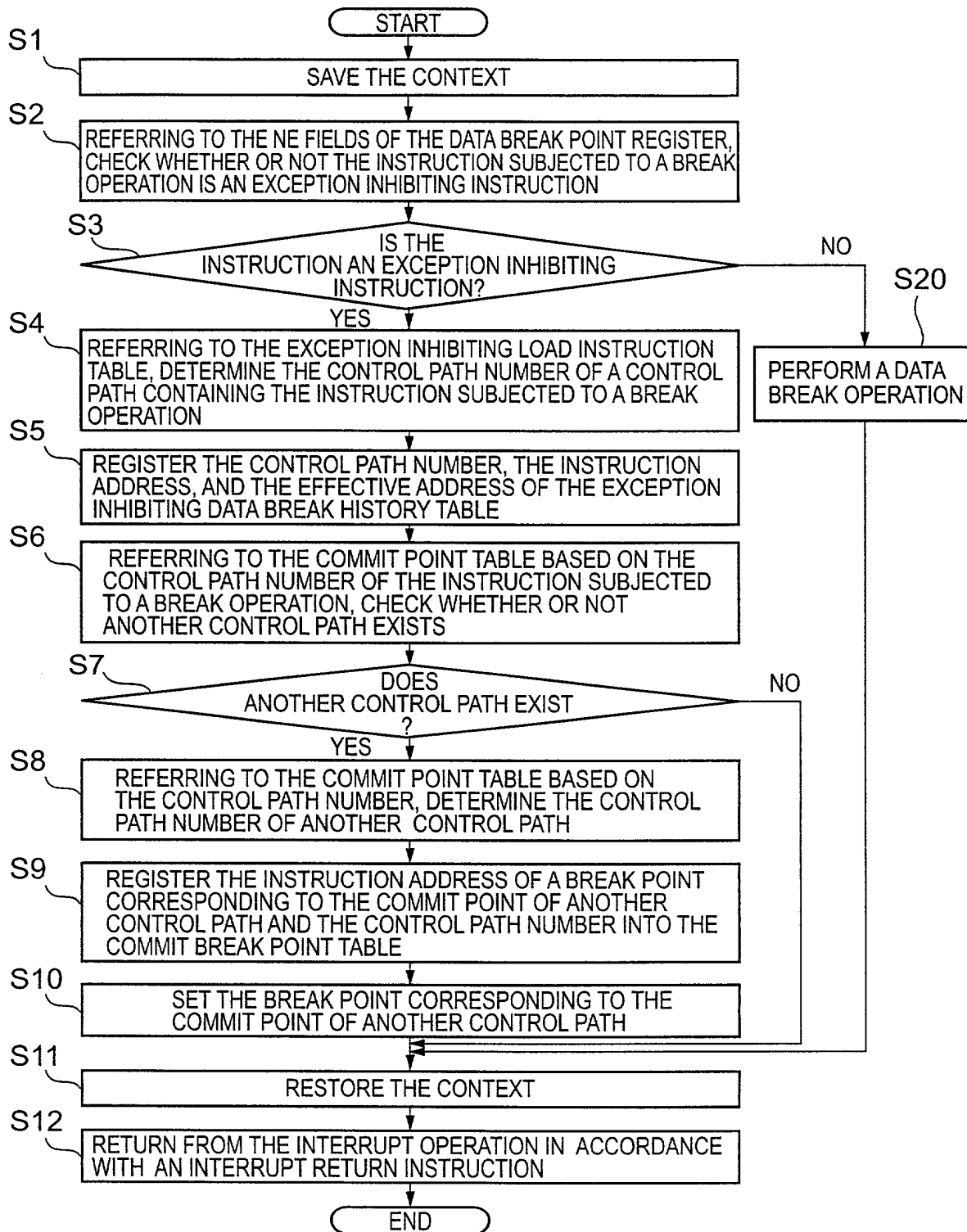


FIG.69



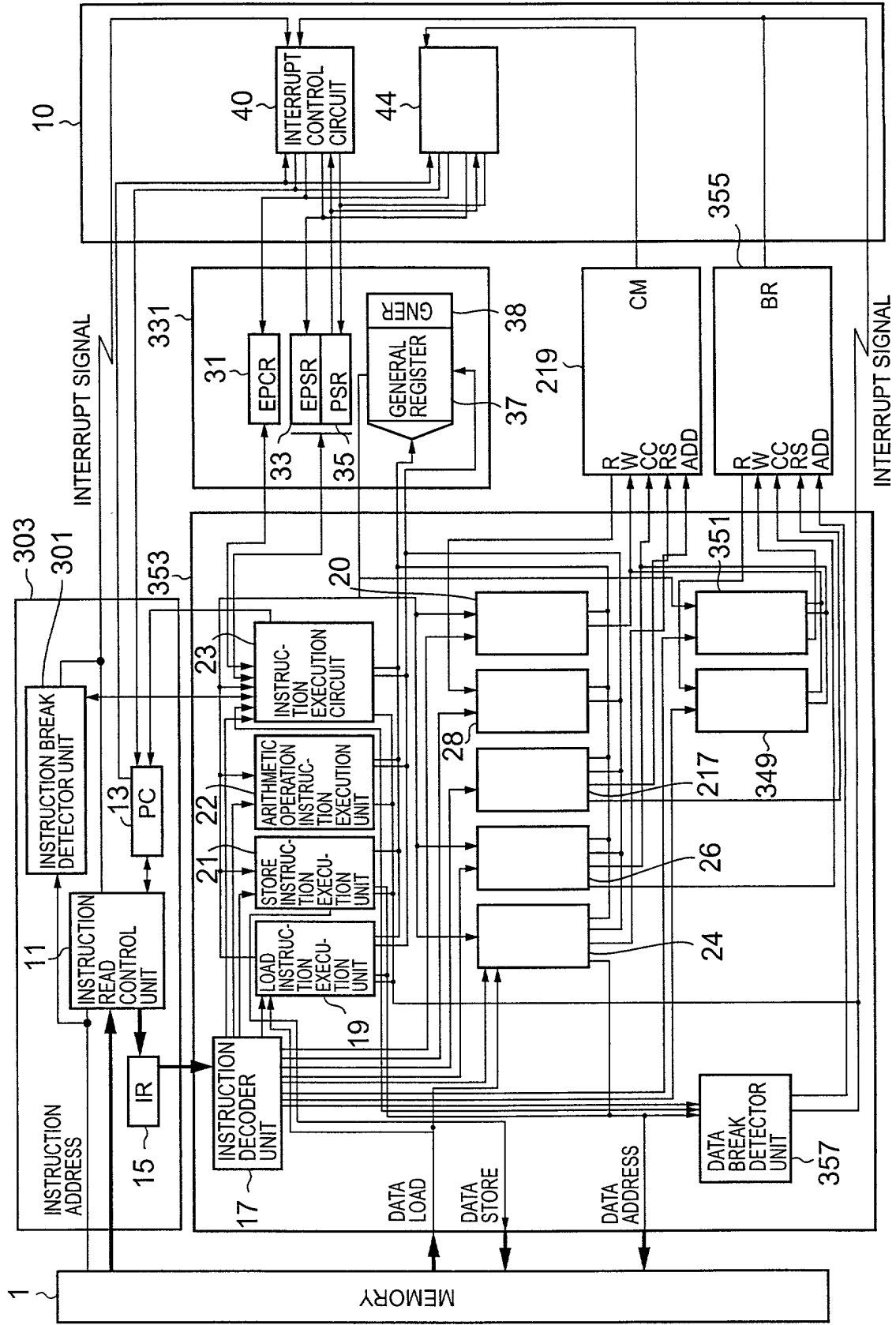


FIG. 71

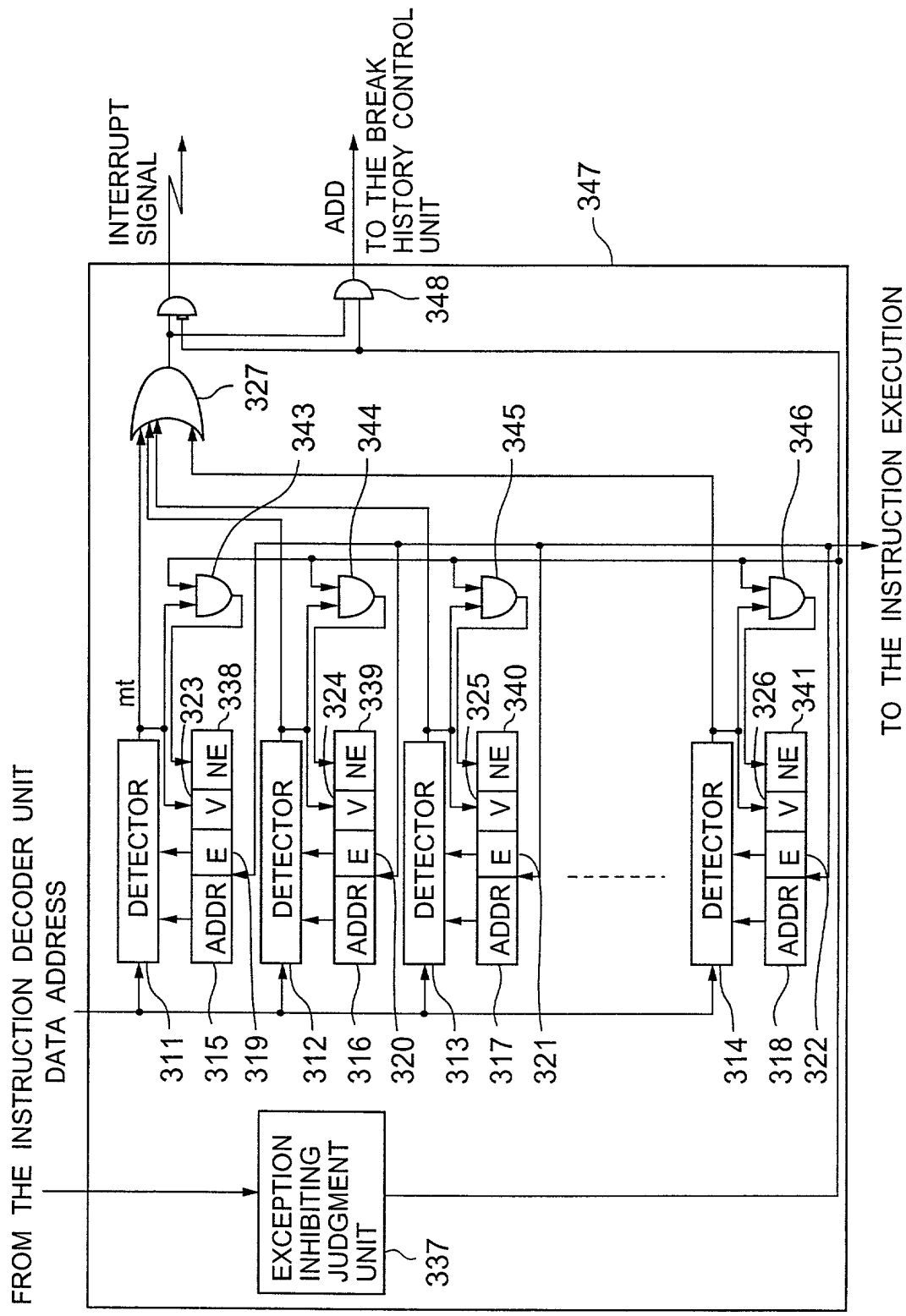


FIG. 72

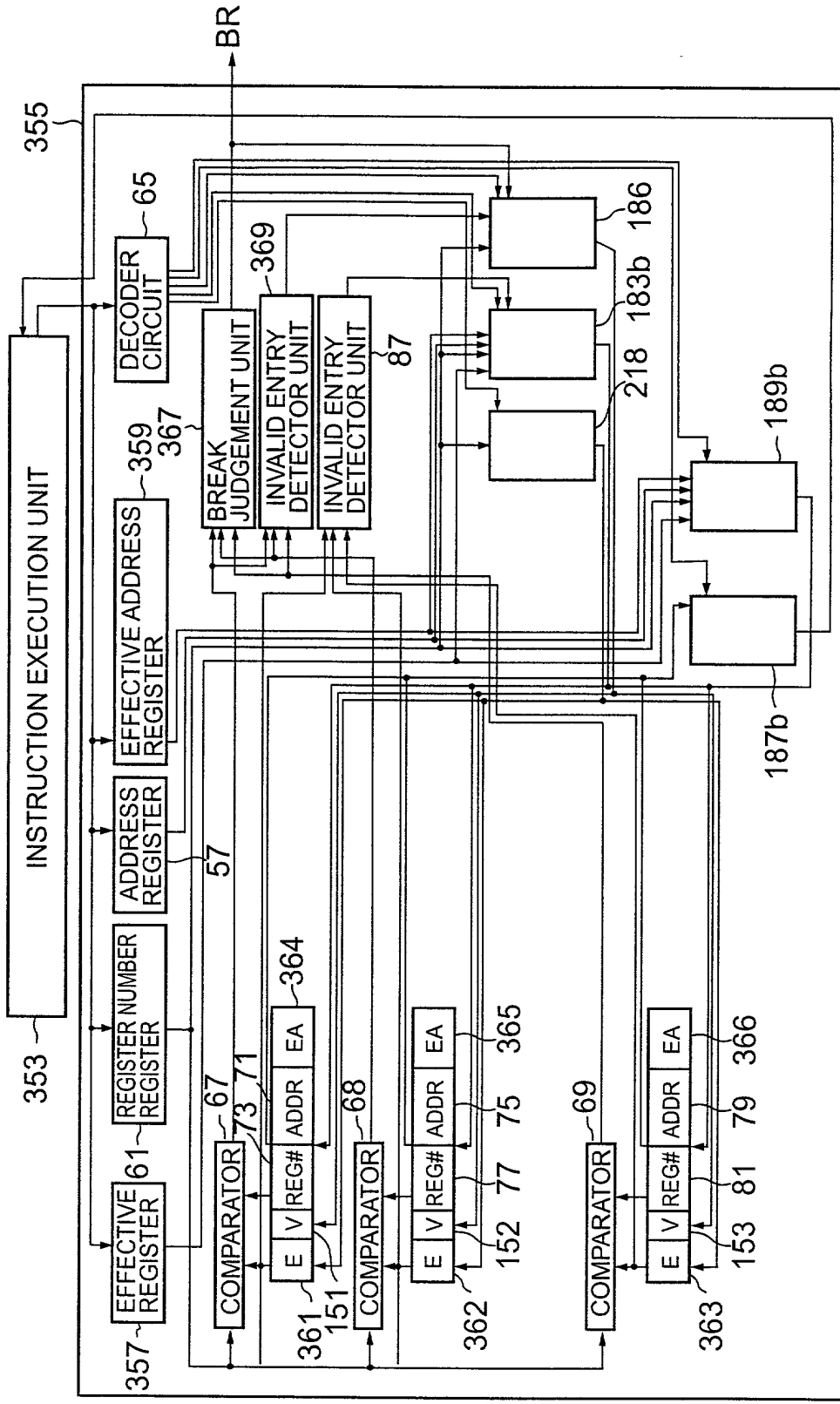


FIG.73

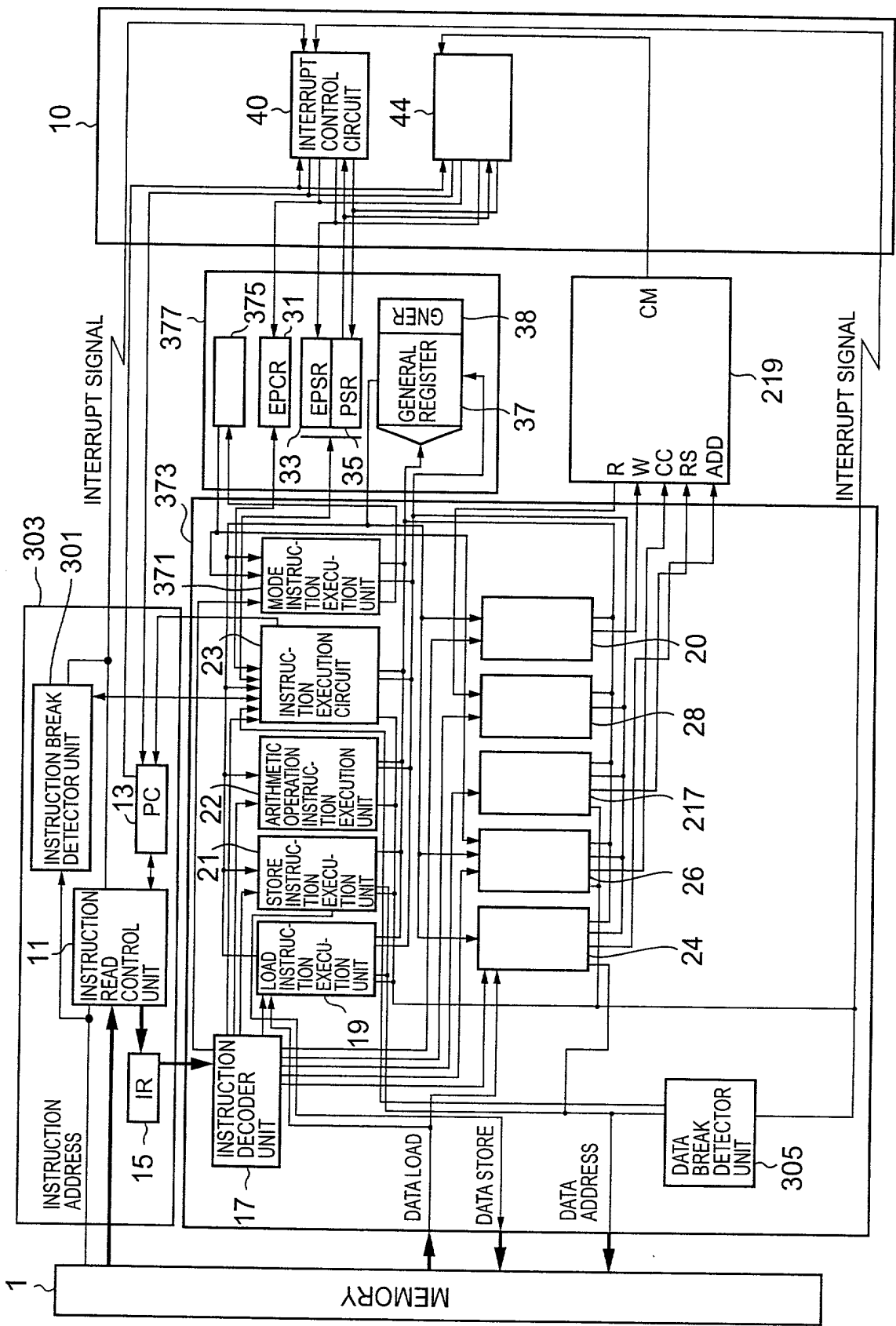


FIG.74

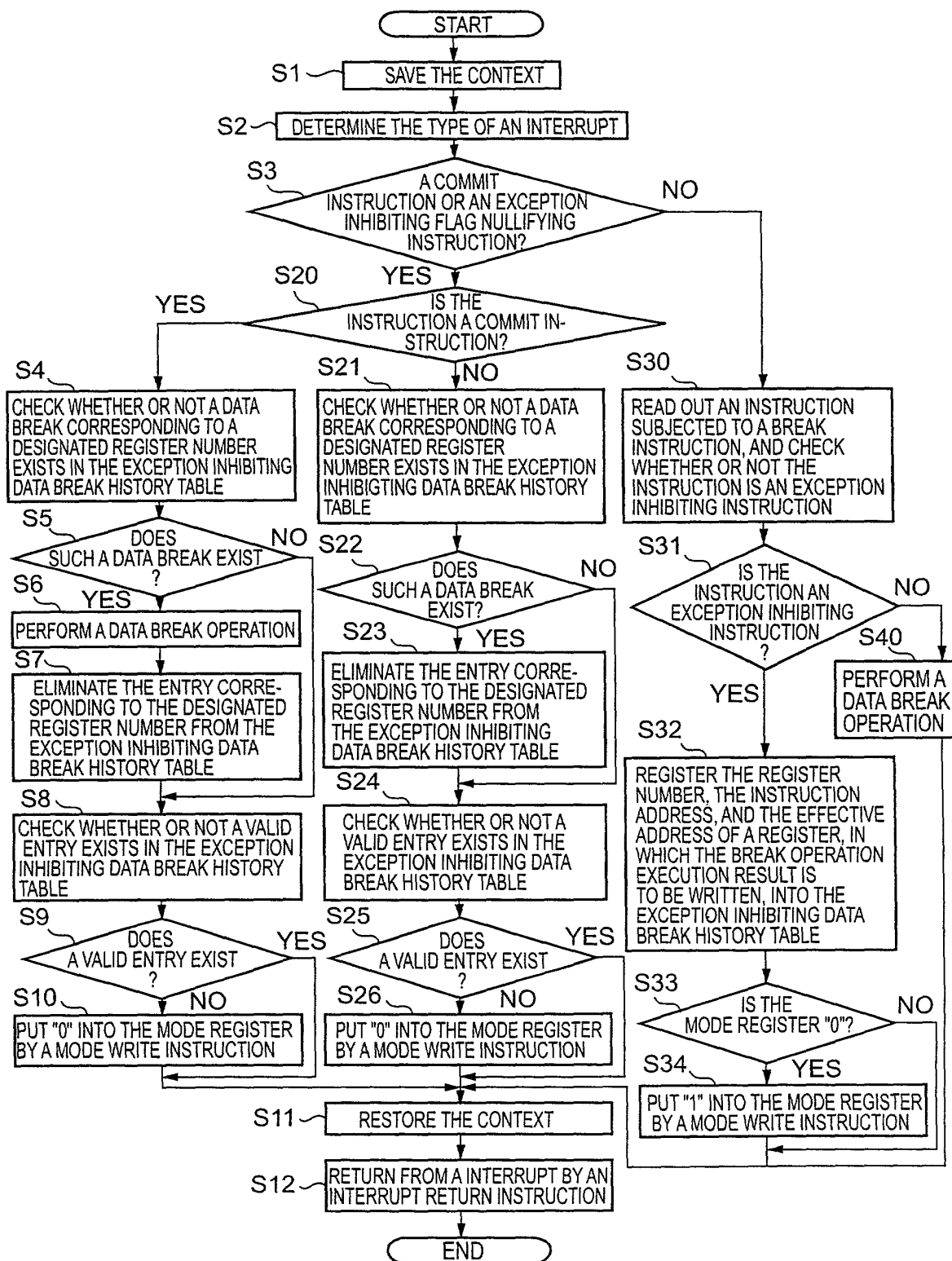


FIG.75

REGISTER NUMBER	INSTRUCTION ADDRESS	EFFECTIVE ADDRESS
r0	a0	ea0
r1	a1	ea1
:	:	:
:	:	:
rl	al	ea1